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Interfacing 7 Series FPGAs High-Performance I/O Banks with 2.5V and 3.3V I/O Standards

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Summary

The I/Os in Xilinx® 7 series FPGAs are classified as either high range (HR) or high performance (HP) banks. HR I/O banks can be operated from 1.2V to 3.3V, whereas HP I/O banks are optimized for operation between 1.2V and 1.8V. In circumstances that require an HP 1.8V I/O bank to interface with 2.5V or 3.3V logic, a range of options can be deployed. This application note describes methodologies for interfacing 7 series HP I/O banks with 2.5V and 3.3V systems.

Interfacing Options

There are different options for interfacing depending on performance needs, function, and signal type (input, output, or bidirectional). This application note explores options such as added resistors, field effect transistor (FET) switches, level translators, and even other Xilinx FPGAs.

Resistive Pull-Down Divider

A simple resistor load can truncate excessive signal swing to tolerable levels for the FPGA. By placing a resistor from the transmission line to GND, as shown in Figure 1, only the driving-High voltage is attenuated. This solution can lead to less than ideal signal integrity because the pull-down resistor is not typically matched to the transmission line. Placing this pull-down resistor close to the receiver helps reduce unwanted reflections.

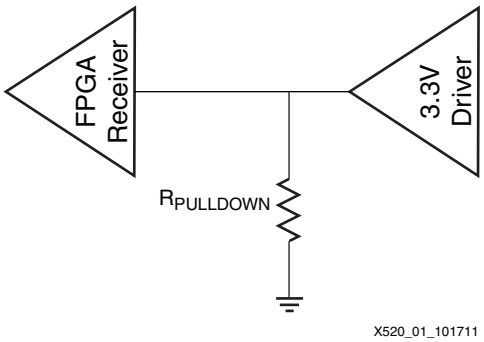

Figure 1: **Example: Pull-Down Resistor Topography**

The pull-down resistor can be determined by knowing the output driver impedance/resistance and output drive voltage (V_{CC}). With the desired receiver input voltage defined as $V_{RECEIVER}$, the pull-down resistor is calculated using Equation 1 along with the effective schematic in Figure 2, page 2.

$$R_{PULLDOWN} = \frac{Z_{DRIVER} \times V_{RECEIVER}}{V_{CC} - V_{RECEIVER}} \quad \text{Equation 1}$$

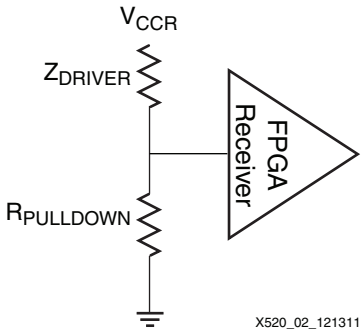

Figure 2: **Effective Schematic of Driver Driving Logic 1 with Pull-Down Resistor**

Table 1 shows calculated values for $R_{PULLDOWN}$ for driver V_{CC} of 2.5V and 3.3V across various driver impedances/resistances.

Table 1: **Calculated Values for $R_{PULLDOWN}$**

Driver V_{CC} (V)	Z_D (Ω)	Receiver V_{CC} (V)	$R_{PULLDOWN}$ (Ω)
2.5	30	1.8	77.1
2.5	40	1.8	102.8
2.5	50	1.8	128.5
2.5	60	1.8	154.3
3.3	30	1.8	36
3.3	40	1.8	48
3.3	50	1.8	60
3.3	60	1.8	72

Due to the potential non-linearity of the driver, it is advised to simulate via HSPICE to take the non-linearity into account. In addition, overshoot and reflections must be accounted for due to the mismatch in impedances. V_{CCOMAX} for the HP I/O bank is 2.1V.

Totem-Pole Resistive Divider

A two-resistor totem-pole solution allows the termination to match the transmission line to minimize reflections, but at the expense of continuous DC current.

The resistors must be chosen such that their combined parallel resistance is as close to Z_0 as possible. In addition, V_{IH} and V_{IL} levels of the receiver must be adhered to. The concept of a V_{BIAS} point, as shown in Figure 3, ensures that the incoming High signal is able to drive down with enough strength to match the drive strength of the incoming Low signal. Knowing this V_{BIAS} point enables calculations for the pull-up and pull-down resistor values. Place the termination resistors close to the receiver for optimum signal integrity.

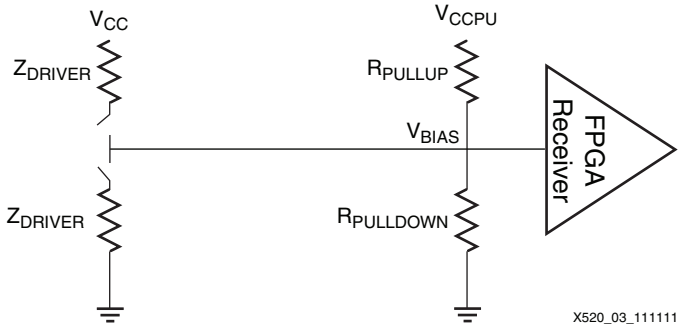

Figure 3: **Schematic of Driver with Thevenin Parallel Termination**

The calculation for V_{BIAS} (Equation 2) is more involved, and assumes that the output High and Low drive strengths are balanced.

$$V_{BIAS} = \frac{V_{CCDRIVER} \times (V_{IL} - margin)}{V_{CCDRIVER} + (V_{IL} - margin) - (V_{IH} + margin)} \quad \text{Equation 2}$$

After V_{BIAS} is obtained, R_{PULLUP} and $R_{PULLDOWN}$ can be calculated as shown in Equation 3:

$$R_{PULLUP} = \frac{V_{CCPU} \times Z_0}{V_{BIAS}} \qquad R_{PULLDOWN} = \frac{Z_0 \times R_{PULLUP}}{R_{PULLUP} - Z_0} \quad \text{Equation 3}$$

Table 2 shows calculated values for R_{PULLUP} and $R_{PULLDOWN}$ for driver V_{CC} of 2.5V and 3.3V.

Table 2: **Calculated Values for R_{PULLUP} and $R_{PULLDOWN}$**

Driver V_{CC} (V)	Z_0 (Ω)	Margin (mV)	V_{IH} (V)	V_{IL} (V)	V_{BIAS} (V)	V_{CCPU} (V)	R_{PULLUP} (Ω)	$R_{PULLDOWN}$ (Ω)
2.5	50	300	1.17	0.63	0.606	1.8	148.5	75.4
3.3	50	300	1.17	0.63	0.504	1.8	178.6	69.4

Using the topography in Figure 3, the output impedance of the driver must be small enough to reach the V_{IH} and V_{IL} thresholds of the receiver. In addition, the output impedance must be large enough not to overdrive the recommended operating voltage (V_{IHMAX}) of the receiver. In 7 series FPGAs, V_{IHmax} for LVCMOS18 is 2.1V. The calculations for $Z_{DRIVER(MAX)}$ and $Z_{DRIVER(MIN)}$ are shown in Equation 4 and Equation 5, respectively.

$$Z_{DRIVER(MAX)} \leq \left(\frac{(V_{CCDRIVER} - V_{BIAS}) \times Z_0}{(V_{IH} + margin) - V_{BIAS}}\right) - Z_0 \quad \text{Equation 4}$$

$$Z_{DRIVER(MIN)} \leq \left(\frac{(V_{CCDRIVER} - V_{BIAS}) \times Z_0}{V_{IHMAX} - V_{BIAS}}\right) - Z_0 \quad \text{Equation 5}$$

Table 3 shows calculated values for $Z_{DRIVER(MAX)}$ and $Z_{DRIVER(MIN)}$ for driver V_{CC} of 2.5V and 3.3V.

Table 3: **Calculated Values for Z_{DRIVER} (Maximum) and Z_{DRIVER} (Minimum)**

Driver V_{CC} (V)	Z_0 (Ω)	Margin (mV)	V_{IH} (V)	V_{IHMAX} (V)	V_{BIAS} (V)	$Z_{DRIVER(MAX)}$ (Ω)	$Z_{DRIVER(MIN)}$ (Ω)
2.5	50	300	1.17	2.1	0.606	59.6	13.4
3.3	50	300	1.17	2.1	0.504	94.7	37.6

At $Z_{DRIVER(MAX)}$, there is exactly 300 mV of margin for logic 1 and logic 0. As the output impedance is reduced, the logic 1 margin grows faster than the logic 0 margin. Equation 6 and Equation 7 calculate exact margin levels depending on actual driver impedance.

$$\text{Logic 1 Margin} = \frac{(V_{CCDRIVER} - V_{BIAS}) \times Z_0}{Z_0 + Z_{DRIVER}} + V_{BIAS} - V_{IH} \quad \text{Equation 6}$$

$$\text{Logic 0 Margin} = V_{IL} + \frac{V_{BIAS} \times Z_0}{Z_0 + Z_{DRIVER}} - V_{BIAS} \quad \text{Equation 7}$$

Table 4 shows calculated values for logic 0 and logic 1 margins for driver V_{CC} of 2.5V and 3.3V.

Table 4: **Calculations for Logic 0 and Logic 1 Margins**

Driver V_{CC} (V)	Z_0 (Ω)	V_{IH} (V)	V_{IL} (V)	V_{BIAS} (V)	Z_{DRIVER} (Ω)	Logic 1 Margin (mV)	Logic 0 Margin (mV)
2.5	50	1.17	0.63	0.606	59.6	300	300
2.5	50	1.17	0.63	0.606	13.4	930	502
3.3	50	1.17	0.63	0.504	94.7	300	300
3.3	50	1.17	0.63	0.504	37.6	930	414

The bias power consumed per I/O from the totem pole termination is calculated using Equation 8, with V_{CC} representing the pull-up voltage.

$$Power = \frac{V_{CC}^{2}}{R_{PULLDOWN} + R_{PULLUP}} \qquad \text{Equation 8}$$

Table 5 shows calculated values for power per I/O based on R_{PULLUP} and $R_{PULLDOWN}$ values from Table 2, page 3.

Table 5: **Calculations for Power per I/O**

Driver V_{CC} (V)	R_{PULLUP} (Ω)	$R_{PULLDOWN}$ (Ω)	V_{CCPU} (V)	Power per I/O (mW)
2.5	148.5	75.4	1.8	14.4
3.3	178.6	69.4	1.8	13.1

By using a parallel termination to V_{BIAS}, the same performance can be achieved with no DC bias at the cost of an additional power rail (Figure 4). If the application has a large number of inputs, this solution could be a more power-efficient option.

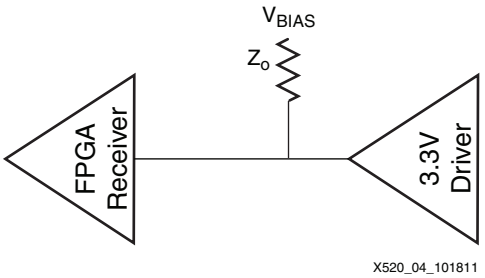

Figure 4: **Example: Parallel Termination to V_{BIAS} Topology**

Series FET Switch

A series FET switch can provide guaranteed unidirectional voltage translation from 3.3V to 1.8V and can be modified to work from 1.8V to 3.3V. The device performs like an NMOS transistor in series with the transmission line, as shown in Figure 5.

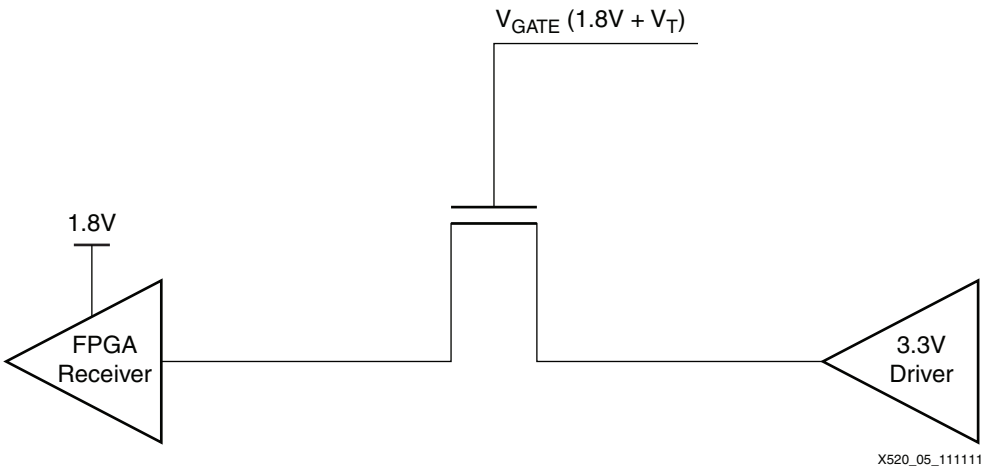

Figure 5: **Series FET Switch**

If the gate of the transistor is set to 1.8V+V_T, the signal from the 3.3V driver only passes up to 1.8V to the receiver. The Texas Instruments SN74TVC16222ADGVR provides 23 parallel NMOS pass transistors with a common gate, as shown in Figure 6.

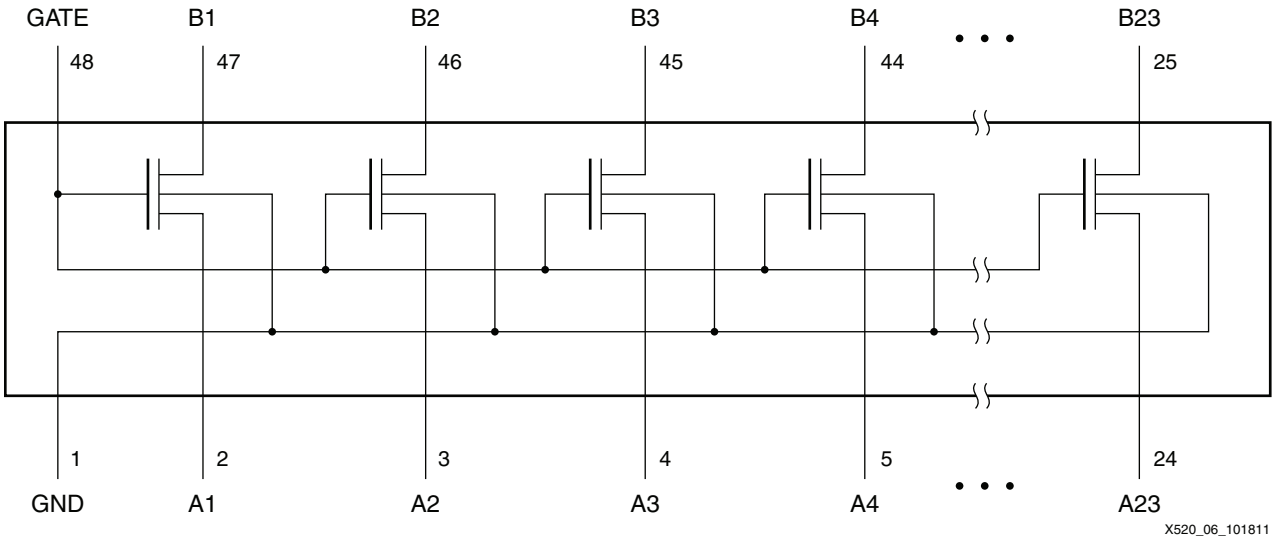

Figure 6: **Simplified Schematic of Texas Instruments SN74TVC16222ADGVR**

To ensure that no more than 1.8V passes through from the 2.5V/3.3V drivers, one of the 23 NMOS transistors can be used to act as a reference transistor to bias all the gate voltages to 1.8V+V_T, as shown in Figure 7.

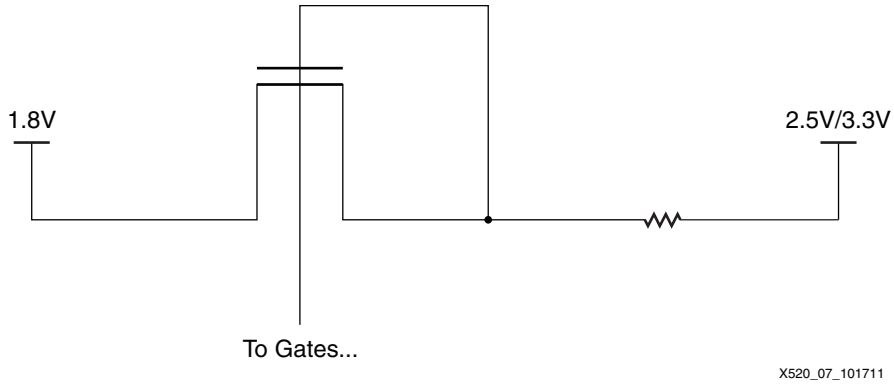

Figure 7: **Reference Transistor Example Set for 1.8V**

The resistor to 2.5/3.3V should be sufficiently high (hundreds of kΩ) to limit the current to the 1.8V rail.

1.8V to 2.5V/3.3V Interface with a FET Switch

Driving 1.8V to a 2.5V or 3.3V receiver via only a FET switch leaves either very little or no V_{IH} margin. In the case of 1.8V driving to, for example, a Spartan®-6 FPGA LVCMOS25 receiver with V_{IH} of 1.7V, only 100 mV of margin is available. In the case of 1.8V driving to a Spartan-6 FPGA LVCMOS33 receiver with V_{IH} of 2.0V, there is no margin at all.

A pull-up resistor at the input to the receiver, as shown in Figure 8, can be used to add margin to the Low-to-High transition signal. Place R_{PULLUP} close to the receiver for optimum signal integrity.

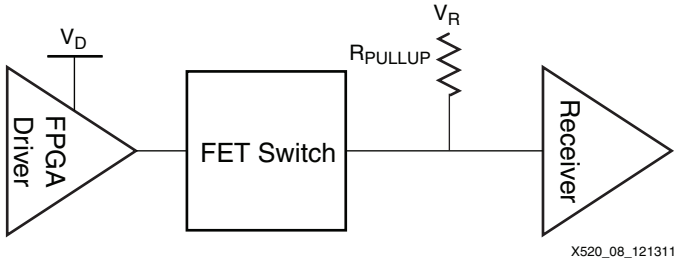

Figure 8: **FET Switch Pull-Up Topography**

Special care must be taken in sizing this resistor because making it stronger helps the Low-to-High transition signal at the expense of the High-to-Low transition signal. In addition, this resistor affects the timing of both Low-to-High and High-to-Low transition signals.

The extra time (T) required to charge the line from V_{CC} of the FPGA driver to V_{IH} (plus margin) can be reasonably estimated in Equation 9 with the topographies shown in Figure 8 and Figure 9. V_{IH} is of the receiver, and V_m is the desired margin above V_{IH}. τ is the time constant R_{PULLUP} x (C_{FET} + C_{LOAD}).

$$T = -\tau \times \ln\left(\frac{V_R - V_{IH} - V_{MARGIN}}{V_R - V_D}\right) \qquad \text{Equation 9}$$

Table 6: **Extra Time to Charge-up through Pull-up Resistor**

V_R (V)	V_D (V)	V_{IH} (V)	V_{MARGIN} (mV)	C_{FET} (pF)	C_{LOAD} (pF)	C_{TOT} (pF)	R_{PULLUP} (Ω)	τ (ns)	Time (ns)
2.5	1.8	1.7	300	4.47	4	8.47	200	1.69	0.57
2.5	1.8	1.7	300	4.47	4	8.47	360	3.05	1.03
2.5	1.8	1.7	300	4.47	4	8.47	500	4.24	1.42
2.5	1.8	1.7	300	4.47	4	8.47	1,000	8.47	2.85
3.3	1.8	2.0	300	4.47	4	8.47	200	1.69	0.69
3.3	1.8	2.0	300	4.47	4	8.47	360	3.05	1.24
3.3	1.8	2.0	300	4.47	4	8.47	500	4.24	1.72
3.3	1.8	2.0	300	4.47	4	8.47	1,000	8.47	3.43

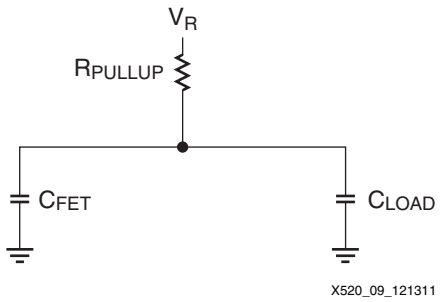

Figure 9: **Schematic Representation of the 3.3V Side of the FET**

The presence of the pull-up resistor affects the High-to-Low transition signal, so the driver impedance must be low enough to ensure that the V_{IL} level is still met, minus some amount of margin. Equation 10 calculates the maximum driver impedance and uses the schematic in Figure 10 as reference.

$$Z_{DRIVER} = \frac{(V_{IL} - V_{MARGIN}) \times R_{PULLUP}}{V_{CC} - (V_{IL} - V_{MARGIN})} \quad \text{Equation 10}$$

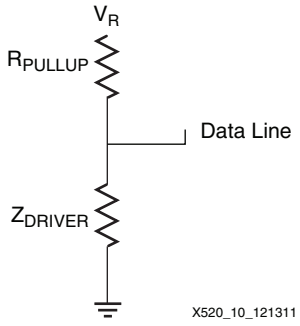

Figure 10: **Schematic of Driver Driving Logic 0 with Pull-up Resistor**

Table 7 shows maximum driver impedance values based on various pull-up resistor values.

Table 7: **Maximum Driver Impedance versus Pull-up Resistor**

V_R (V)	V_{IL} (V)	V_{MARGIN} (mV)	R_{PULLUP} (Ω)	Z_{MAX} (Ω)
2.5	0.8	300	200	50
2.5	0.8	300	360	90
2.5	0.8	300	500	125
2.5	0.8	300	1,000	250
3.3	0.8	300	200	35
3.3	0.8	300	360	64
3.3	0.8	300	500	89
3.3	0.8	300	1,000	179

I2C Compatibility

Using the FET switch with the proper resistor pull-up value can successfully level translate I2C signals.

Automatic Level Translator

The Texas Instruments TXB0108 block diagram in Figure 11 is an automatic direction sensing level translator. The ability to automatically sense the direction of traffic makes an automatic level translator easy to drop into a bidirectional system. There are no additional control signals because each bit has an independent directional sensor. This device adds up to 7.6 ns of propagation delay to the circuit (3.3V to 1.8V). Due to the nature of this device, if termination or other heavy loading is present on the line, logic faults could result. Termination and bus loads must be greater than 50 kΩ to avoid logic interruptions. For this reason, open drain buses such as I2C and 1Wire are not compatible with this type of level translator.

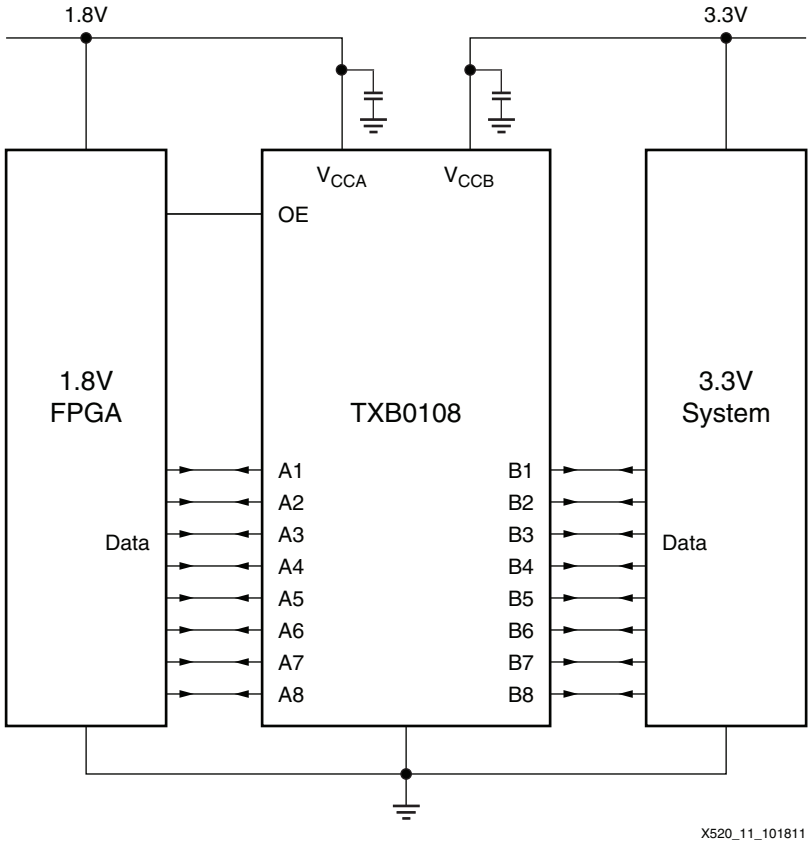

Figure 11: **Automatic Level Translator Topology**

Directional Level Translator

The Texas Instruments SN74AVC20T245 is a 20-bit bidirectional level translator that level-shifts data from A to B or B to A (Figure 12, page 10) depending on the logic of DIR.

The SN74AVC20T245 is broken into two 10-bit buses, each with independent DIR control. There is also an output enable for each block to isolate port A from B. A pin-to-pin propagation delay of up to 4.6 ns exists through the device.

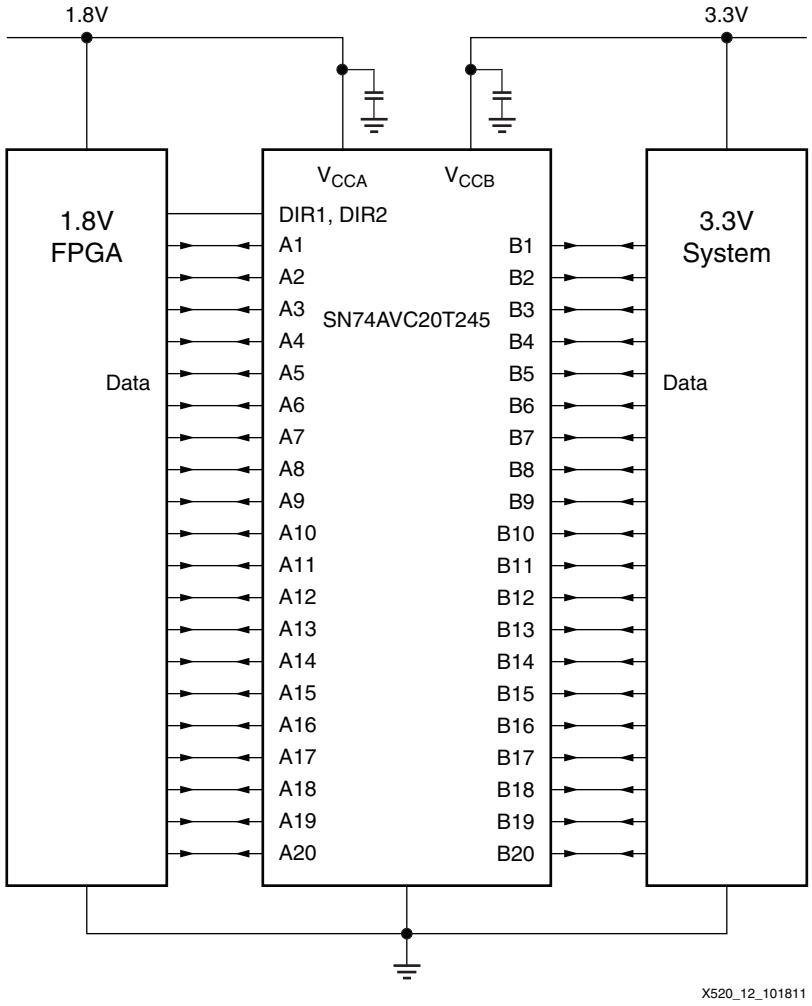

Figure 12: **20-Bit Bidirectional Level Translator Topography**

CPLDs and FPGAs

A variety of Xilinx devices are 2.5V and 3.3V tolerant and can be fitted for bidirectional level-shifting applications.

Xilinx CPLDs are ideally suited for level-shifting to/from 3.3V, and are available with up to 117 I/O to support up to a 58-bit bus. Spartan-6 FPGAs are also well-suited for level-shifting to/from 3.3V and are available with up to 530 I/O. Virtex-6 FPGAs are also viable options, with level-shifting to/from 2.5V. The non-volatile Spartan-3AN family is another viable option.

Using CPLDs or FPGAs allows for off-loading of other logic and tasks from the 7 series FPGAs. Pin-to-pin propagation delay through a Xilinx CPLD is 5 ns, while for FPGAs it is dependent on routing through the devices.

Inside a CPLD or Spartan device (Figure 13), an IOBUF is instantiated to interface with the 7 series device, while another IOBUF is used to interface with the 2.5V/3.3V logic. A signal is brought into the device from either the 7 series FPGA or the 3.3V logic to identify the direction of traffic.

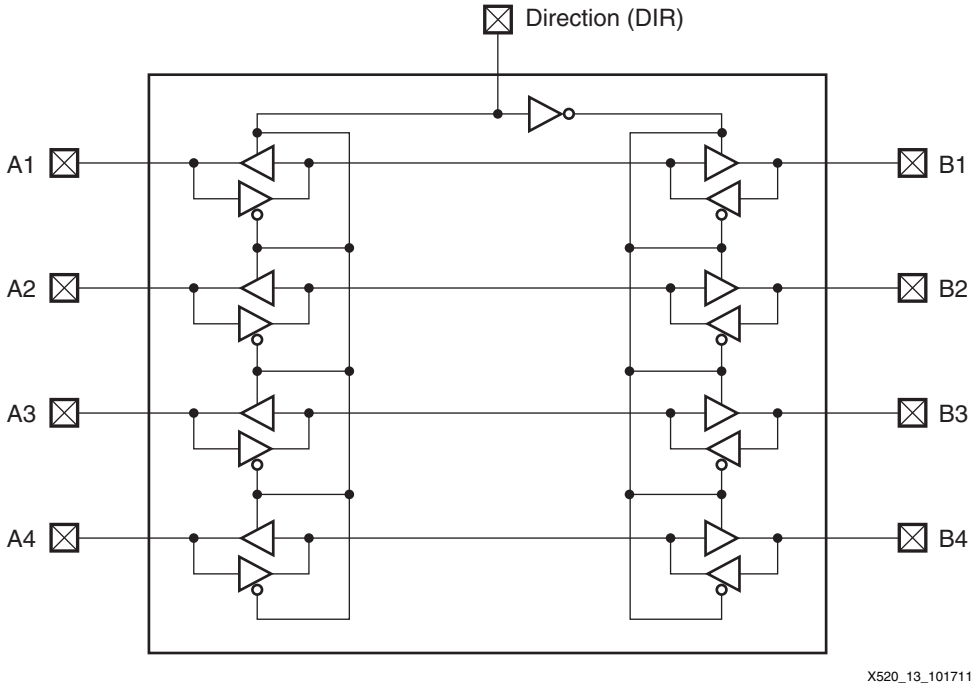

Figure 13: **Example Schematic of CPLD or FPGA Design**

Design Guidelines

Table 8 summarizes the various interface methodologies described in this application note.

Table 8: **Comparison of Design Guidelines**

Type	External Part Numbers	Bit Width	Bidirectional	Input	Output	Bus Must Be Aligned to Directional Signal (DIR)	Supports Open Drain Drivers	Supports Termination	Number of Components	Propagation Delay (ns)
Resistive Pull-Down Divider	N/A	N/A	No	Yes	No	No	Yes	Yes	1	N/A
Totem-Pole Resistive Divider	N/A	N/A	No	Yes	No	No	Yes	Yes	2	N/A
Series FET Switch	SN74TVC16222ADGVR	22	Yes(1)	Yes	Yes(1)	No	Yes(4)	Yes	1(2)	0.25
Automatic Level Translator	TXB0108	8	Yes	Yes	Yes	No	No	No	1	7.6
Directional Level Translator	SN74AVC20T245	20	Yes	Yes	Yes	Yes	Yes	Yes	1	4.6
CPLDs and FPGAs	XC9536XL	16(3)	Yes	Yes	Yes	Yes(3)	Yes	Yes	1	5

Notes:

1. Has capability of bidirectional support with a pull-up resistor.
2. Two components if using a pull-up resistor.
3. Bit widths are dependent on device size.
4. Includes I2C with suitable pull-up resistor.

Conclusion

The high-performance I/O banks in the 7 series FPGAs are able to accommodate higher voltage interfaces via a series of options that can accommodate virtually all design, cost, and performance needs.

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
12/13/11	1.0	Initial Xilinx release.

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