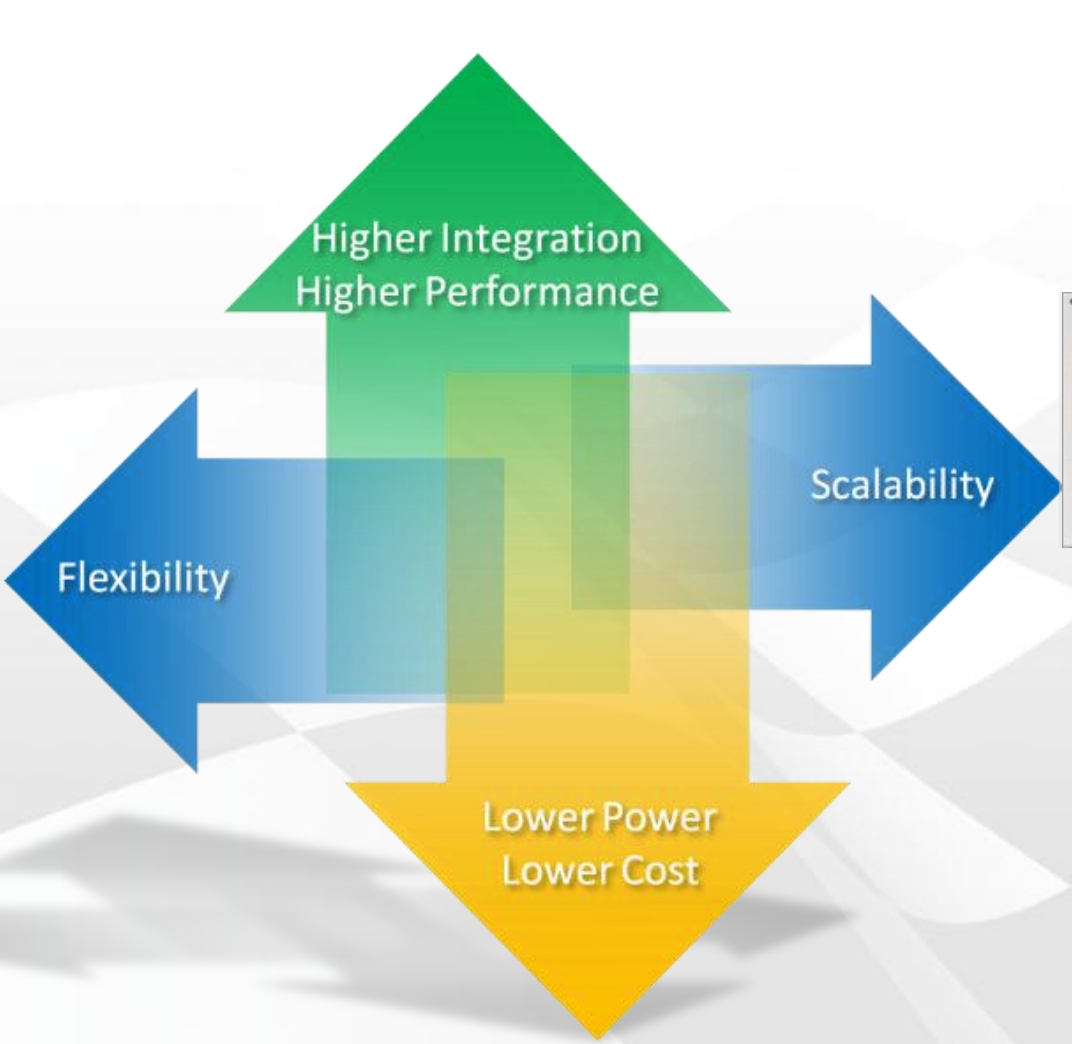
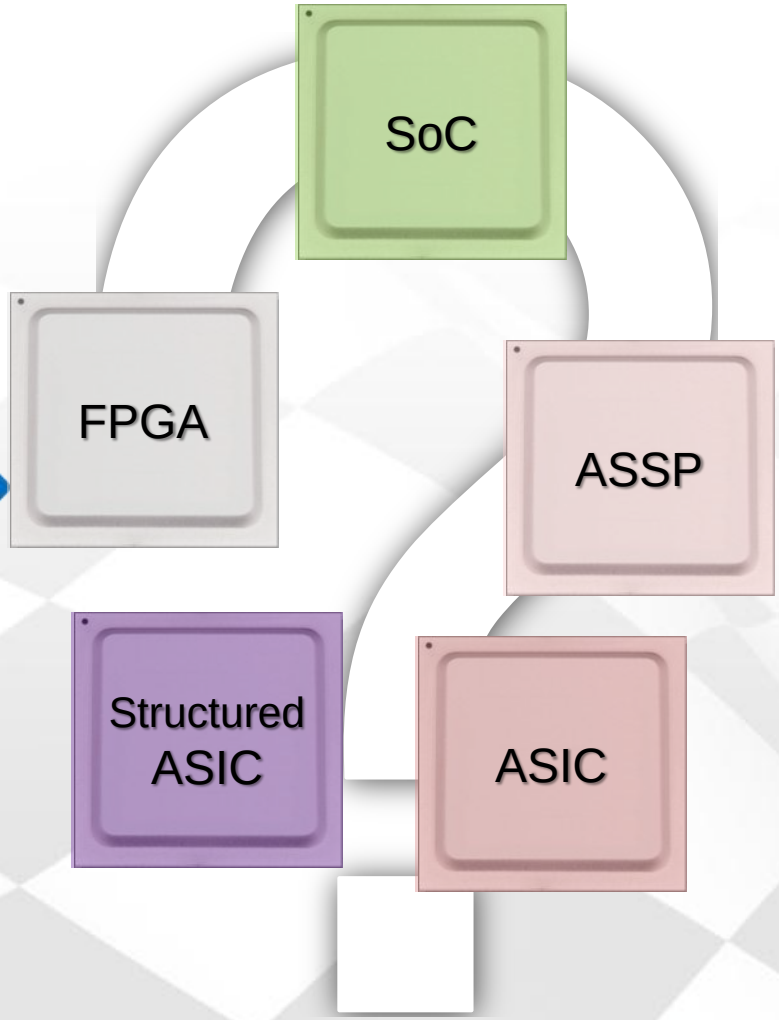
Introduction to Xilinx Zynq-7000™ All Programmable SoC

Agenda

- **Embedded Processor Challenge**
- Zynq-7000 AP SoC Family Overview
- Zynq-7000 AP SoC Ecosystem
- Zynq-7000 AP SoC HW & SW Design Tools and Flow
- Zynq-7000 AP SoC Development Kits, Training, and Docs

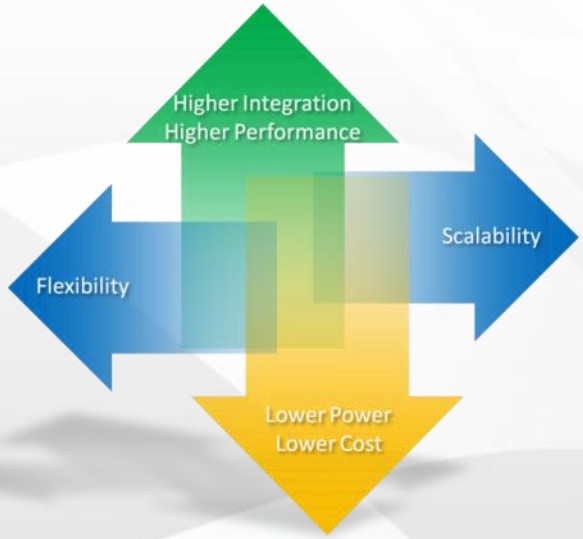
Embedded Processor Challenge





Which Technology Should I Choose?

Zynq-7000 AP SoC Value Proposition



	ASIC	ASSP	2 Chip Solution	Zynq-7000
Performance	+	+	■	+
Power	+	+	-	+
Unit Cost	+	+	-	■
TCO	■	+	+	+
Risk	-	+	+	+
TTM	-	+	+	+
Flexibility	-	-	+	+
Scalability	-	■	+	+

+ positive, - negative, ■ neutral

Conflicting Demands Now Served by the Xilinx Zynq-7000

AVNET electronics marketing

SPEEDWAY DESIGN WORKSHOPS

Course Objectives

- Embedded Processor Challenge
- **Zynq-7000 AP SoC Family Overview**
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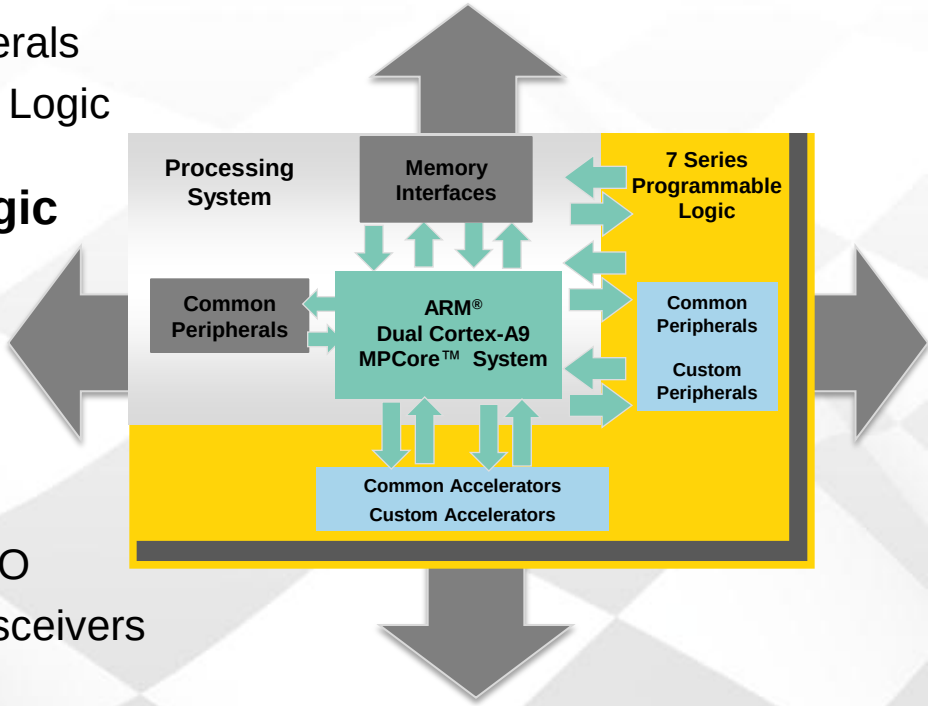
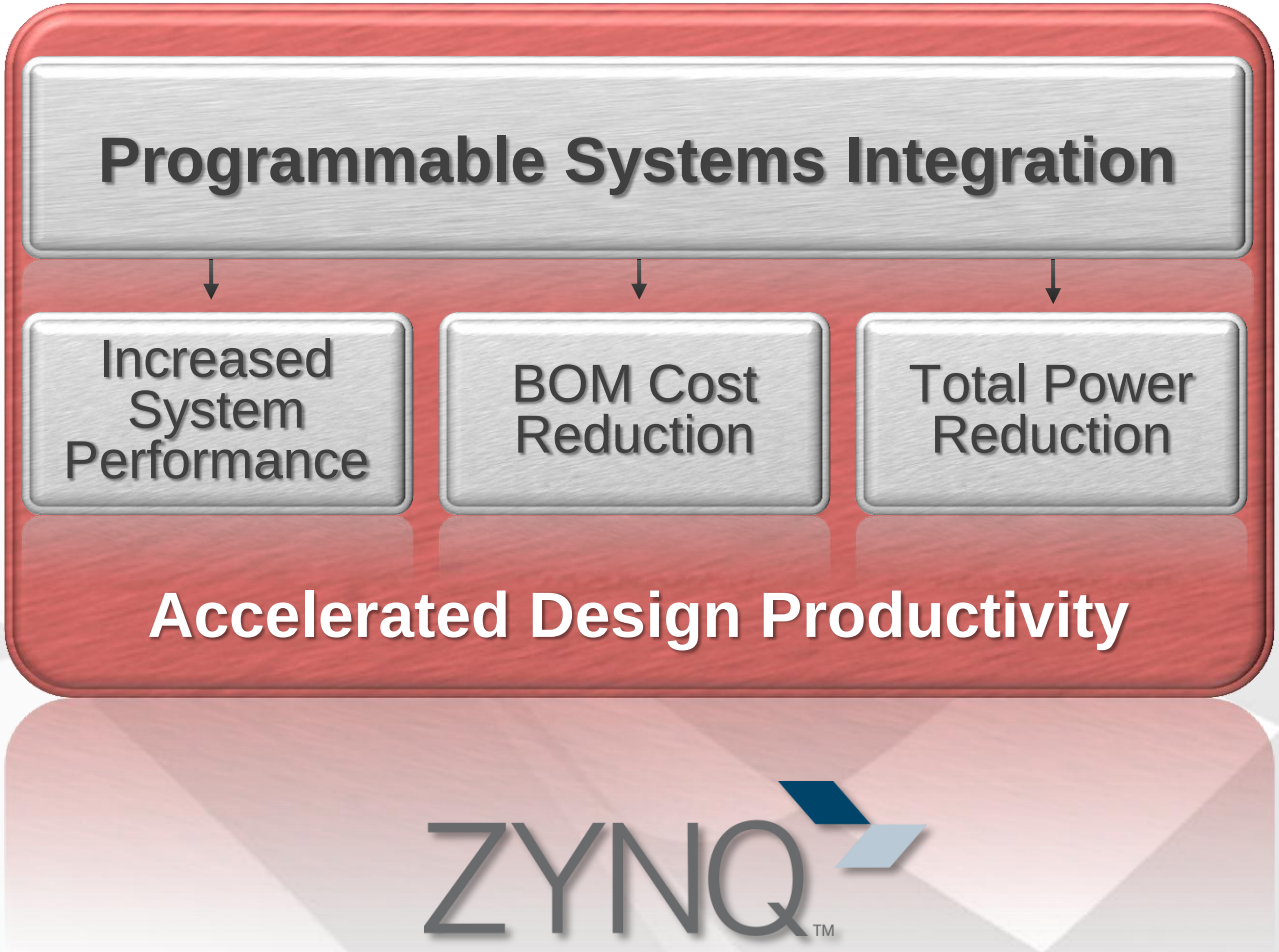
Introducing Xilinx Zynq™-7000 AP SoC

- **Complete ARM®-based Processing System**
  - Dual ARM Cortex™-A9 MPCore™, processor centric
  - Integrated memory controllers & peripherals
  - Fully autonomous to the Programmable Logic
- **Tightly Integrated Programmable Logic**
  - Used to extend Processing System
  - Scalable density and performance
  - Over 3000 internal interconnects
- **Flexible Array of I/O**
  - Wide range of external multi-standard I/O
  - High performance integrated serial transceivers
  - Analog-to-Digital Converter inputs



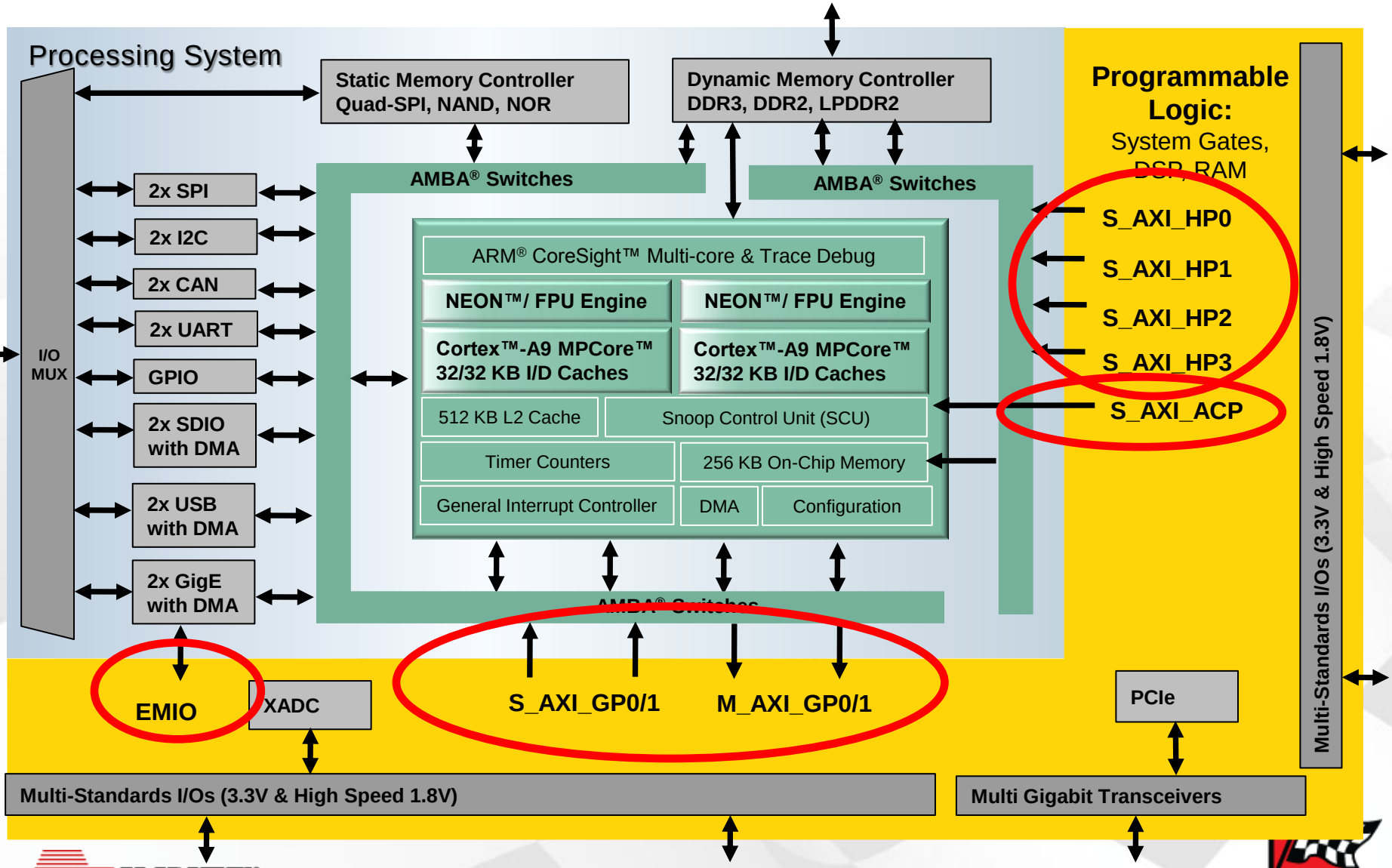
Zynq-7000 can meet customer's expectations



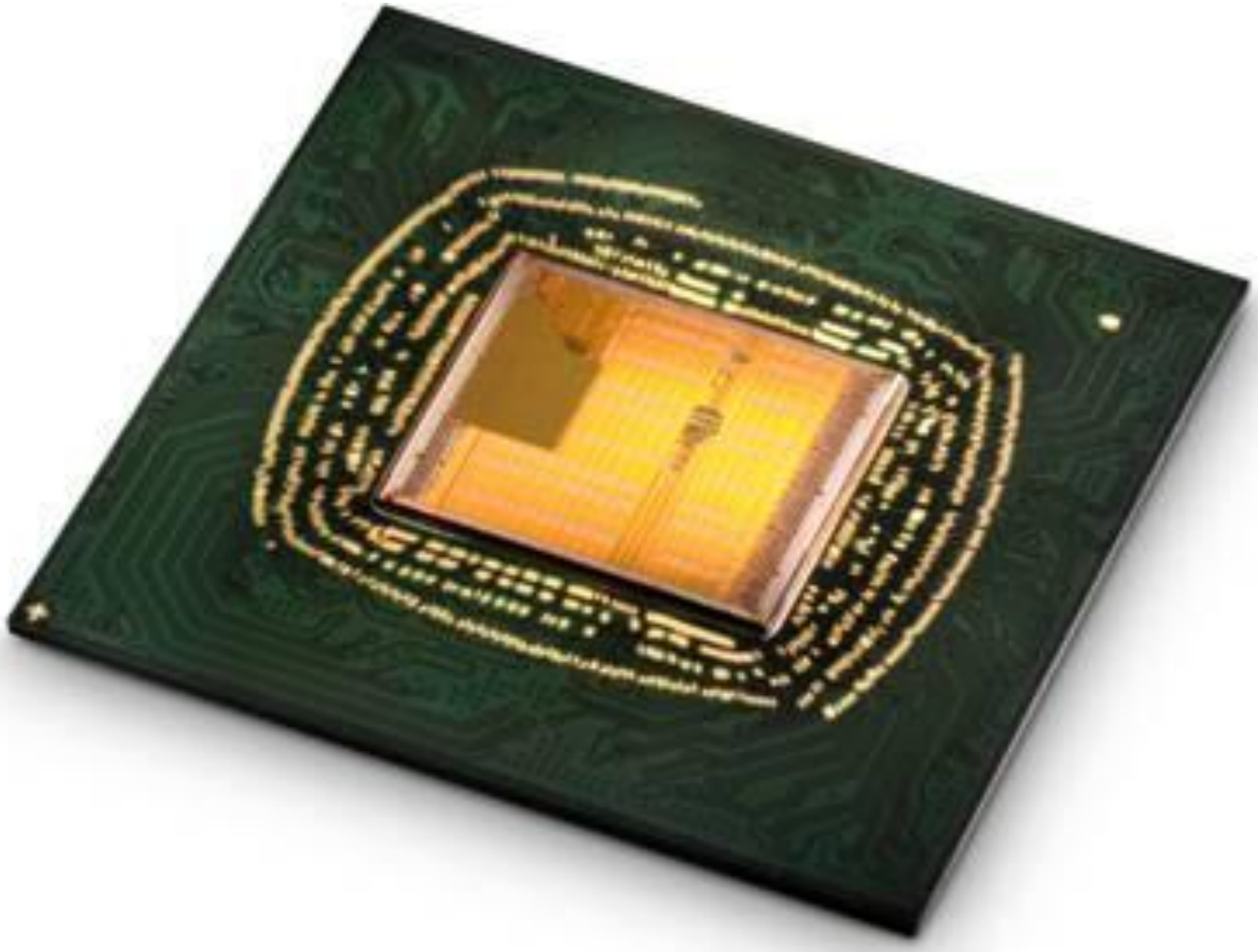
Zynq-7000: Break-out in Customer Value

- **All Programmable + Systems Integration**
  - ARM Cortex™-A9 MPCore™ Processing System with hardened peripherals, ADC and 28nm scalable optimized programmable logic
- **Increased System Performance**
  - Dual Core ARM Cortex A9's with NEON and FPU
  - Programmable logic with massive DSP processing
  - Optimized & Simplified HW/SW Partitioning, HW Accelerator
- **BOM Cost Reduction**
  - Reduced Devices per Board (Processors, PLDs, DSPs, ADC, Power supplies, fans, etc…)
  - Reduced PCB Complexity (Fewer traces/interconnect/layers, Fewer power supplies，Smaller overall PCB …)
- **Total Power Reduction**
  - Flexible/Tunable Power Envelope
  - Integration Power Reduction
- **Accelerated Design Productivity**
  - Reduced Time To Market (Ecosystem, HLS, Platform, Plug&Play AXI IP …)

Zynq-7000 AP SoC Block Diagram

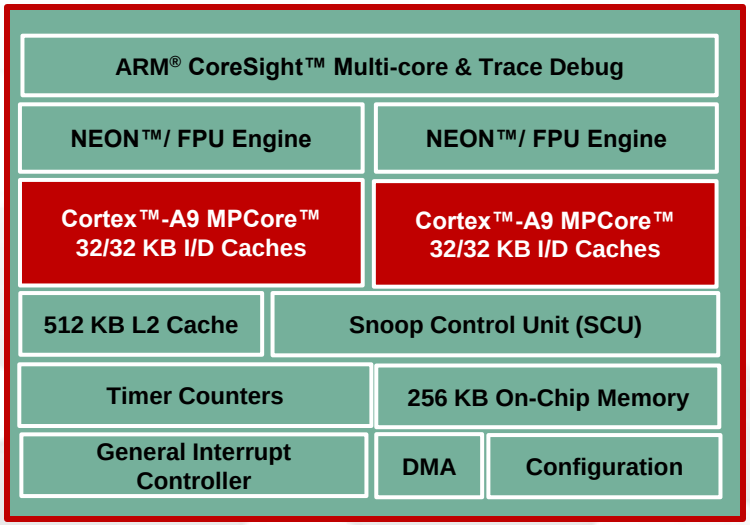


Real Zynq-7000 AP SoC Silicon (XC7Z020)



ARM Cortex-A9 Processor and L1 Caches

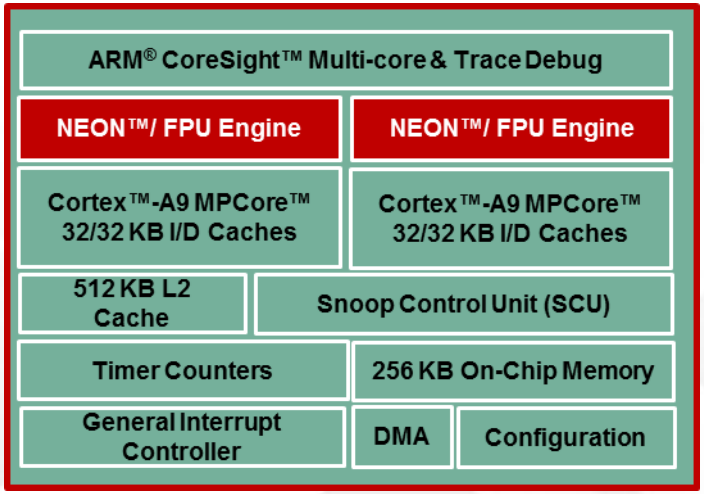
- **ARM Cortex-A9 processor key features**
  - 2.5 DMIPS/MHz or 11.5 CoreMark™/MHz per core
  - Up to 800MHz/1GHz operation
  - Harvard architecture, 64-bit data and 64-bit instruction interfaces
  - Little endian support for both instruction and data

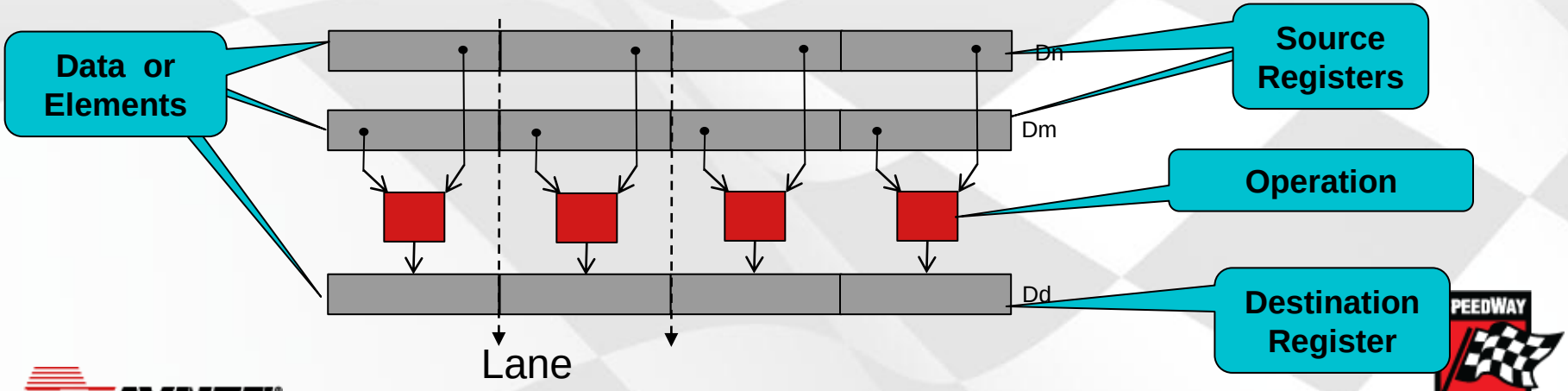


- **ARM Cortex-A9 processor L1 cache key features**
  - 32KB Instruction and 32KB Data cache
  - The cache line length is eight words (32 bytes)
  - 4-way set associative, write-back
  - All L1 caches support parity

NEON

- **NEON technology is wide Single Instruction Multiple Data (SIMD) parallel & co-processing architecture**
  - Extension of ARM instruction set – not a standalone DSP processor
- **Applications**
  - For real-time soft codec performance, able to keep up with evolving Codec standards
  - Video encode/decode
  - 2D/3D graphics,
  - Audio and speech processing,
  - Image processing
- **Fewer cycles needed as compared to ARM CPU only**
  - Rule of thumb: NEON optimizations will half number of cycles for entire codec





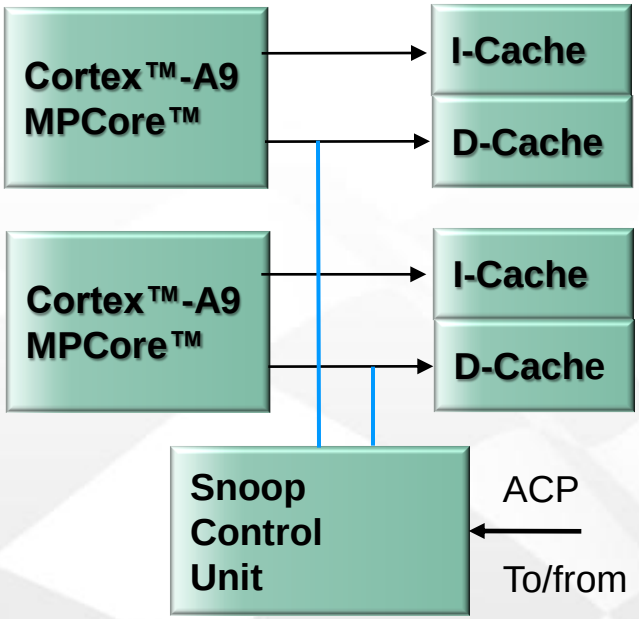
FPU

- **High performance single/double precision VFPv3 FPU**
  - Includes half-precision conversions (FP16) useful for graphics & audio
- **Register set shared with NEON**
  - Requires crafting of NEON and FPU code versus pure FPU code for hand crafted code
  - Expands the size of the FPU register set
- **Compliant with IEEE-754 standard (with noted exceptions)**
- **Floating Point Performance is:**

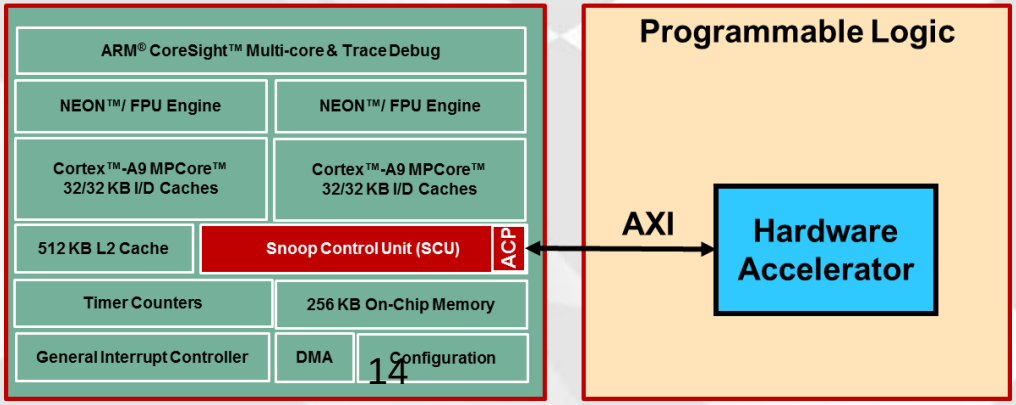
CPU MHz	MFLOPs/MHz*	1 CPU GFLOPs	2 CPU GFLOPs
800	2	1.6	3.2
667	2	1.3	2.7
533	2	1.1	2.1
400	2	0.8	1.6

SCU and ACP

- **Snoop Control Unit (SCU) Features**
  - L1 Cache Snoop Control
    - Coherent option for multi-core software development
    - Snoop filtering monitors cache traffic
    - High performance cache-to-cache transfers
    - Accelerator Coherency Port



- **Accelerator Coherence Port**
  - Accelerators gain access to CPU cache hierarchy
  - Uses AMBA® 3 AXI™ technology for compatibility with standard un-cached
  - Supported in hardware - no software needed
  - Allows coherency to be extended to PL

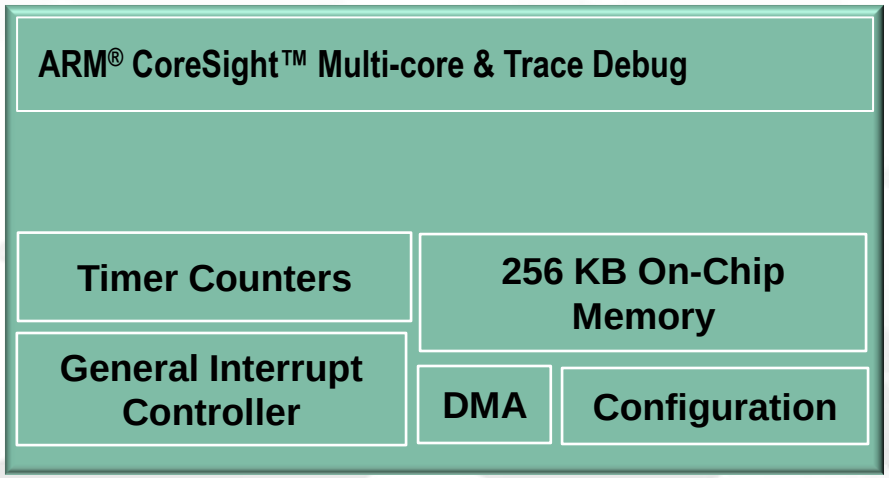


The rest of APU

- **General Interrupt Controller**
  - Ability to route interrupts to either CPU or both CPUs
  - Supports 53 interrupts (16 dedicated to the Programmable Logic)

- **On Chip Memories (OCM)**
  - Boot ROM (not user accessible)
  - 256 KB shared SRAM with parity

- **Central DMA (8 Channels)**
  - 4 for the Processing System
  - 4 for the Programmable Logic
  - Dedicated synchronization signals to PL

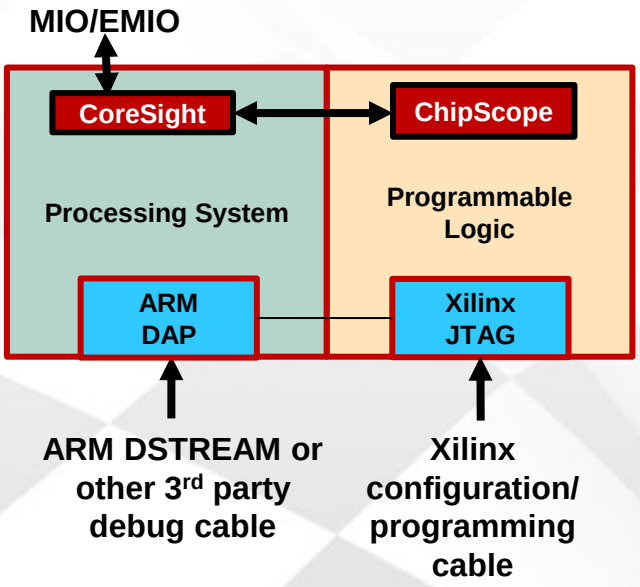


- **Device Configuration (DEVC)**
  - Interface to configure Programmable Logic

- **Private Watch Dog Timer and Timer for each CPU**
- **System Watch Dog and Triple Timer Counters**
- **ARM CoreSight Debug Technology**

Hardware/Software Debug Support

- **One-cable solution (cascaded JTAG)**
  - Xilinx cable connected to the Xilinx JTAG
    - ARM Debug Access Port (DAP) in front of Xilinx JTAG in the chain
    - Software debug with SDK
    - Hardware debug with ChipScope
    - iMPACT bitstream download

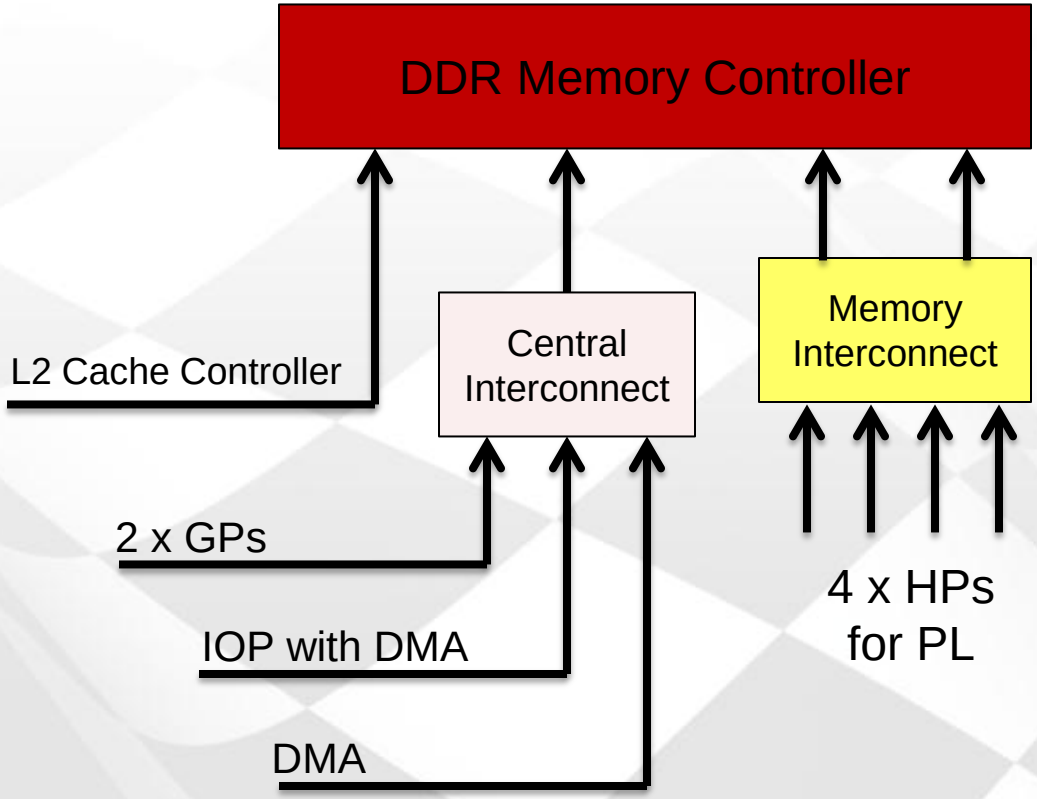


- **Two-cable solution (independent JTAG)**
  - Xilinx cable connected to the Xilinx JTAG
    - Hardware debug with ChipScope
    - iMPACT bitstream download
  - ARM DSTREAM/3rd party cable connected to DAP
    - Software debug using ARM/3rd party tools

- **CoreSight™ (Processor Trace)**
  - 16-bit via MIO, 125MHz internal clock, sampled at both edges of the clock
  - 32-bit via EMIO, 250MHz EMIOTRACECLK, sampled at the rising clock edge

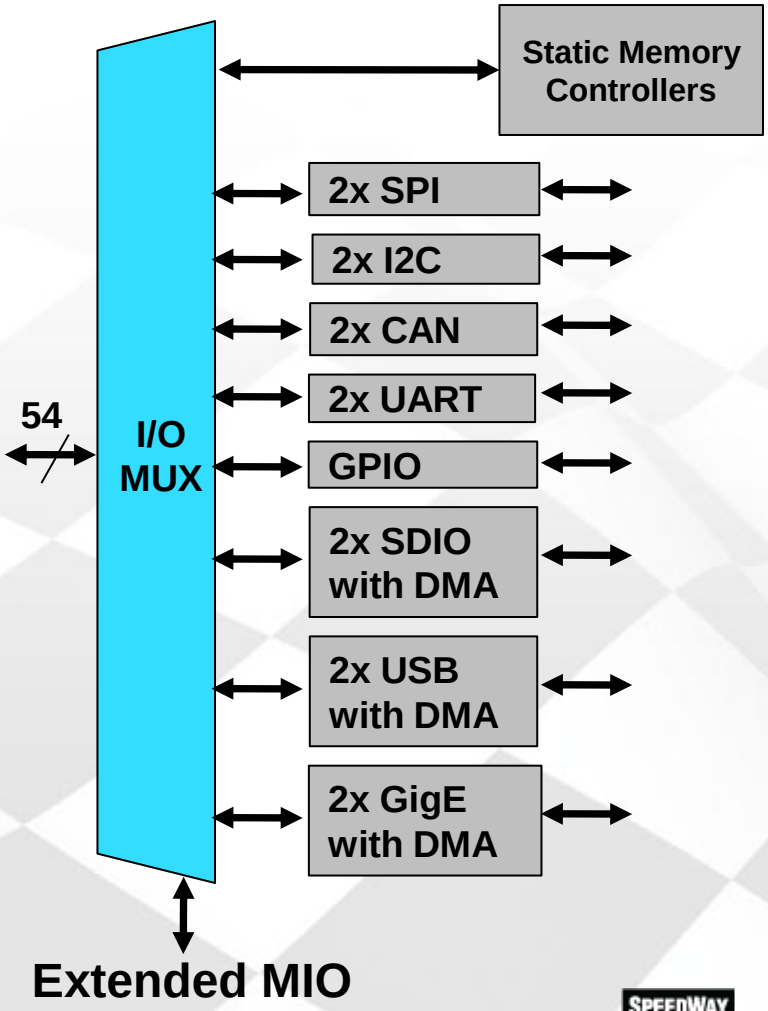
Memory Controller in Zynq-7000

- **DDR controller**
  - DDR3, DDR2, and LPDDR2
  - 16 bit or 32 bit wide; ECC on 16 bit
  - DDR3 @ 1.5V up to DDR1333
  - DDR2 @ 1.8V up to DDR800
  - LPDDR2 @ 1.2V up to DDR800
  - 73 dedicated DDR pins
  - Credit-based round robin arbitration
  - No DIMM support
- **NAND Controller**
  - ECC
  - 8 bit or 16 bit data widths
- **NOR/SRAM Controller**
  - 8 bit data width
- **Quad SPI (QSPI) Controller**
  - Up to 2 QSPI parallel memories



PS Common Peripherals

- **Two USB 2.0 OTG/Device/Host**
  - ULPI, 12 Endpoints
  - Full and High Speed support
- **Two Tri- Mode GigE (10/100/1000)**
  - IEEE1588 rev 2.0
- **Two SD/SDIO interfaces**
  - Memory, IO and combo cards
- **Two CAN 2.0B, SPI , I2C , UART**
- **Four GPIO 32bit Blocks**
- **Multiplexed Input/Output (MIO)**
  - Multiplexed output of peripheral and static memories
  - Two I/O Banks: each selectable - 1.8V, 2.5V or 3.3V
  - Configured using new feature in XPS
- **Extended MIO**
  - Enables use of Select IO with PS peripherals



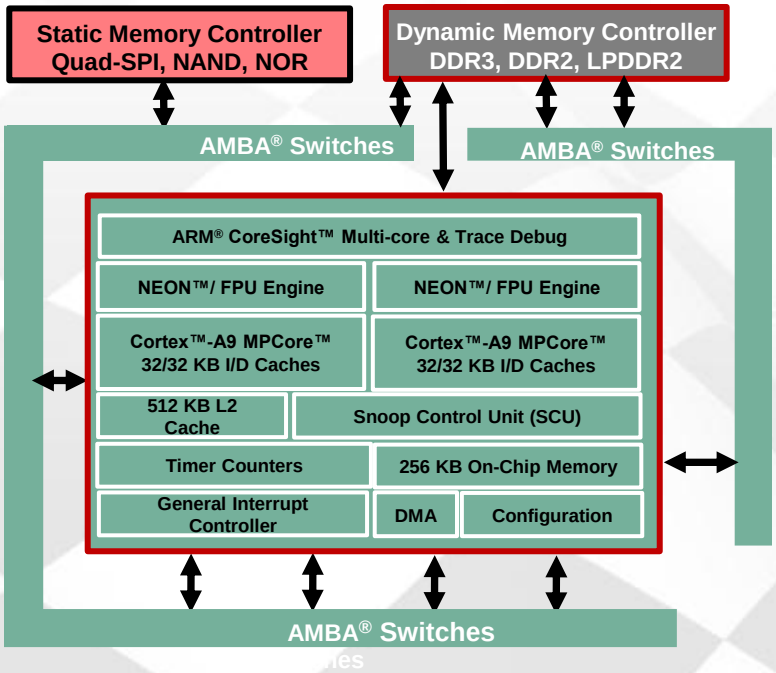
Zynq-7000 Configuration and Boot

- **Processor First! CPU configures the PS and PL**
  - Standalone PL configuration (without PS configuration) is not supported
  - Configuration under external host control is also possible via JTAG

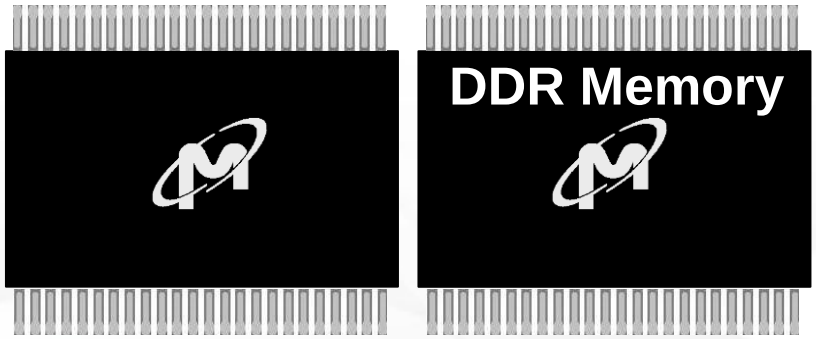
- **Two boot modes**
  - Secure boot
  - Non-secure boot

- **Four master boot methods (secure or non-secure boot)**
  - QSPI (16MB, 50MB/Sec)*
  - NOR (64MB, 20MB/Sec)
  - NAND (tested up to 1GB, 10MB/Sec)*
    - * cannot be used in the same design
  - SD (Up to 32GB)

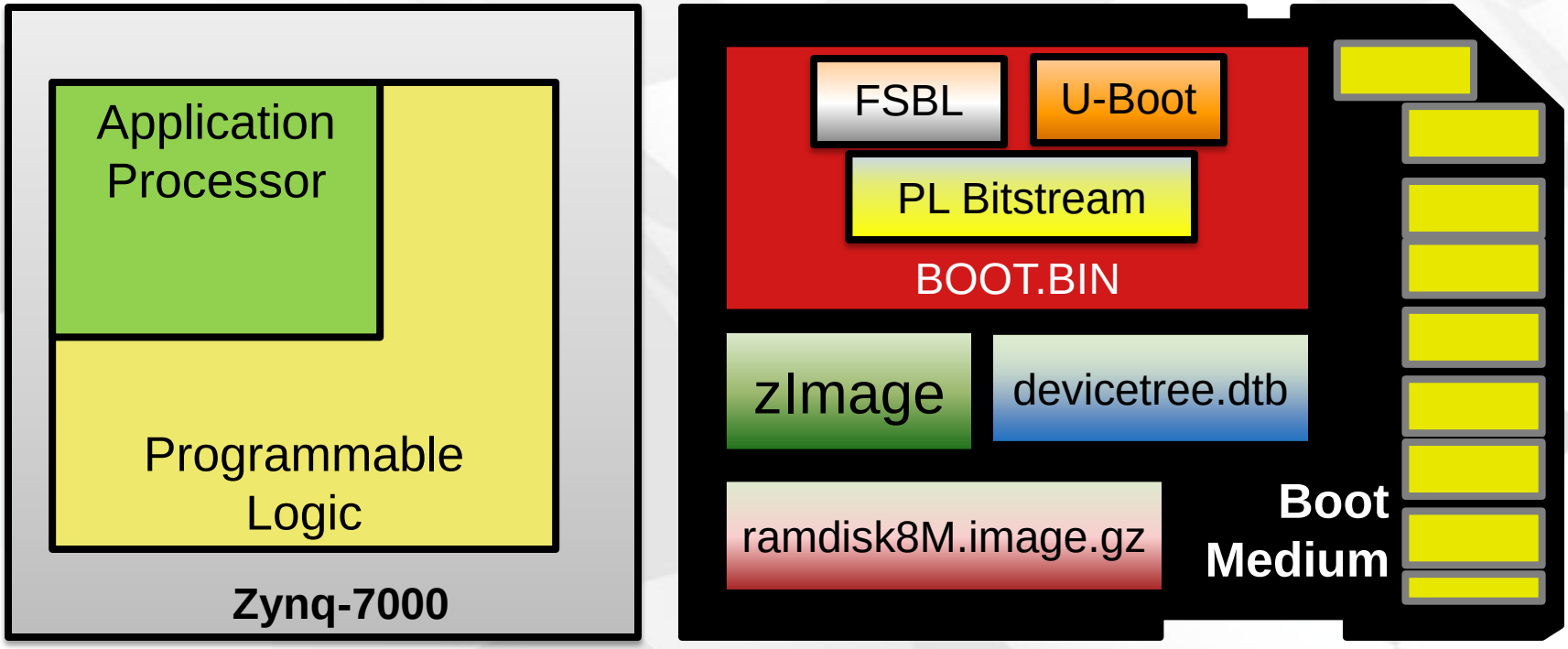
- **One slave boot method (non-secure)**
  - JTAG for debug and development



Booting Linux on Zynq-7000



- **Example of Zynq-7000 booting Linux**
  - BOOT.BIN on SD Card



Zynq-7000 AP SoC Product Table

	Devices Name	Z-7010	Z-7015	Z-7020	Z-7030	Z-7045	Z-7100
	Part Number	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z045	XC7Z100
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™					
	Processor Extensions	NEON™ & Single / Double Precision Floating Point					
	Max Frequency	800MHz			1GHz		
	Memory	L1 Cache 32KB I / D, L2 Cache 512KB, on-chip Memory 256KB					
	External Memory Support	DDR2, DDR3, LPDDR2,2x QSPI, NAND, NOR					
	Peripherals	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 32b GPIO					
Programmable Logic	Logic Architecture	Artix-7 FPGA				Kintex-7 FPGA	
	6-input Look-Up Table (LUT)	17,600	46,200	53,200	78,600	218,600	277,400
	Flip-Flops	35,200	92,400	106,400	157,200	437,200	554,800
	Extensible Block RAM(# of Blocks)	240KB (60)	340KB (95)	560KB (140)	1,060KB (265)	2180KB (545)	3020 KB (545)
	Peak DSP Performance (Symmetric FIR)	100 GMACs	100 GMACs	276 GMACs	593 GMACs	1334 GMACs	2,622 GMACs
	PCI Express® (Root Complex or Endpoint)	Gen2 x 4			Gen2 x4	Gen2 x8	Gen2 x 8
	Analog to Digital Converters (ADC)	Dual 12bit 1Msps A/D Converter					
I/O	Processor System IO	130					
	Multi Standards 3.3V IO	100		200	100	212	
	Multi Standards High Performance 1.8V IO	-			150	150	
	Multi Gigabit Transceivers	-			4	16	

Zynq-7000 AP SoC Package Table

	Devices Name	Z-7010		Z-7015	Z-7020		Z-7030			Z-7045			Z-7100	
	Part Number	XC7Z010		XC7Z015	XC7Z020		XC7Z030			XC7Z045			XC7Z100	
Package	Package Type	CLG225	CLG400	CLG485	CLG400	CLG484	FBG484	FBG676	FFG676	FBG676	FFG676	FFG900	FFG900	FFG1156
	Package Size (mm)	13 x 13	17 x 17	19 x 19	17 x 17	19 x 19	23 x 23	27 x 27	27 x 27	27 x 27	27 x 27	31 x 31	31 x 31	35 x 35
	Pitch (mm)	0.8	0.8	0.8	0.8	0.8	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
	PS MIOs	32	54	54	54	54	54	54	54	54	54	54	54	54
	HR IO (1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V)	54	100	150	125	200	100	100	100	100	100	212	212	250
	HP IO (1.2V, 1.35V,1.5V,1.8V)	-	-	-	-	-	63	150	150	150	150	150	150	150
	Serial Transceiver	-	-	4	-	-	4	4	4	8	8	16	16	16
	Max Transceiver Speed	N/A	N/A	5.4 Gbps	N/A	N/A	6.6 Gbps	6.6 Gbps	12.5 Gbps	6.6 Gbps	12.5 Gbps	12.5 Gbps	10.3 Gbps	10.3 Gbps

Zynq-7000 AP SoC Temperature Range

	-1C	-1I	-2I	-2E	-3E	-1Q
Z-7010	yes	yes	yes	yes	yes	no
Z-7015	yes	yes	yes	yes	yes	no
Z-7020	yes	yes	yes	yes	yes	yes
Z-7030	yes	yes	yes	yes	yes	yes
Z-7045	yes	yes	yes	yes	yes	yes
Z-7100	yes	yes	yes	yes	yes	N.A

C Grade ➔ 0C to +85C
E Grade ➔ 0C to +100C
I Grade ➔ -40C to +100C
Q Grade ➔ -40C to +125C

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- **Zynq-7000 AP SoC Ecosystem**
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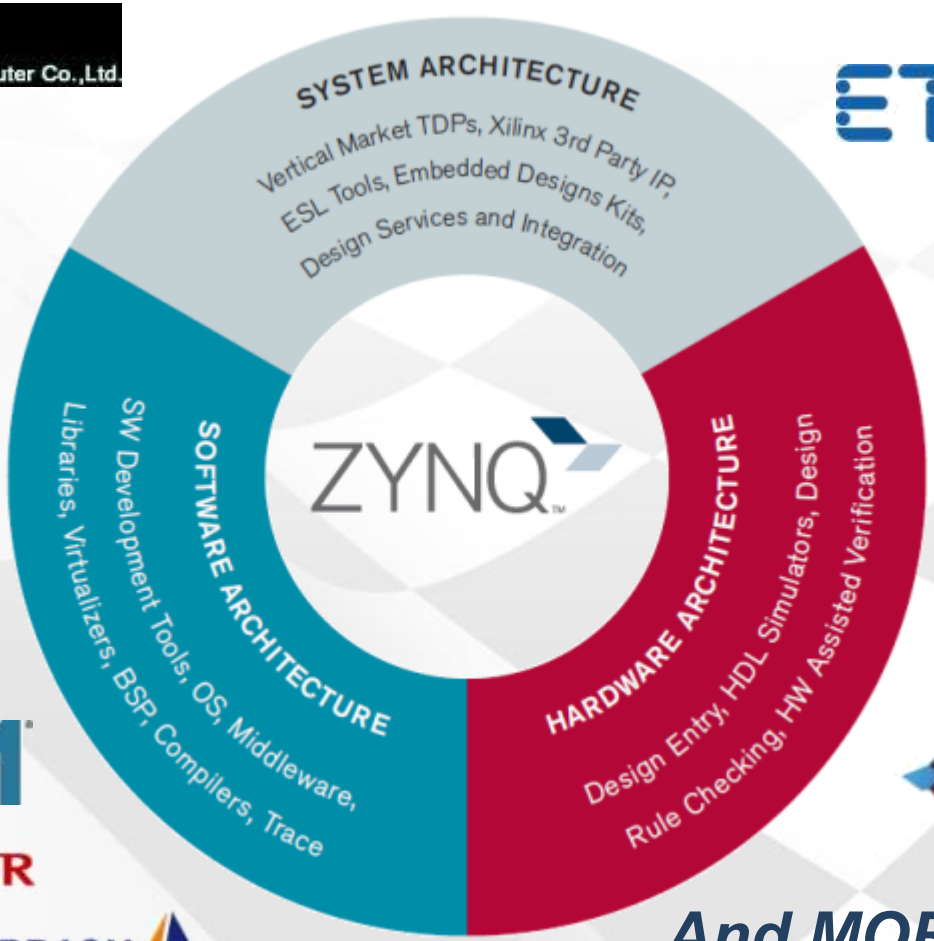
Zynq-7000 Extensive Partnership Ecosystem



Computex

cadence™ vector

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KMC Kyoto Microcomputer Co.,Ltd.

YOKOGAWA

ETAS

iVeia Enabling Small Form Factor Solutions

freeRTOS

eSOL

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Mentor Graphics

petalogix LINUX SOLUTIONS FOR A RECONFIGURABLE WORLD

NATIONAL INSTRUMENTS

ARM

The MathWorks

android

WIND RIVER

LAUTERBACH DEVELOPMENT TOOLS

AVNET electronics marketing

And MORE …

SPEEDWAY DESIGN WORKSHOPS

Operating Systems Support & Status

OS	Provider	Version	Availability (ZC702 board support)	Segment Market
Linux				Used in all segments
ENEA Linux	ENEA	3.0	Now	
WR Linux 5	Wind River	3.4	Now	
MVL CGE6	Montavista	2.6.32	Jan '13	Communications
LinuxLink	Timesys	NA	Now	Industrial, Medical, Automotive
Android	iVeia	2.3	Now	Consumer
Windows Embedded Compact 7	Adeneo Embedded	7	Now	ISM, Automotive
VxWorks	Wind River	6.9.2	Now	ISM, Automotive, A&D
INTEGRITY	GreenHills Software	NA	Now	A&D, Automotive, ISM
QNX	Adeneo Embedded	6.5	April '13	Automotive, ISM
OSE	ENEA	5.5	Now	Communication
ThreadX/NetX	Express Logic	NA	Now	Consumer, Medical, Industrial
FreeRTOS	Xilinx	7.x	Now	All segments
RTA-OS SC1-4	ETAS	3.0	Now (single core)	Automotive
eCOS	ITR	3.0	Q4CY2012	ISM, Automotive
eT-Kernel	eSOL	TBD	Now	Automotive, Consumer
µc/OS	Micrium	II	Now	Industrial, Medical, A&D
Nucleus	Mentor	NA	Now	Industrial, Medical and Automotive
Quadros	Quadros	NA	Now	Industrial, Medical, POS

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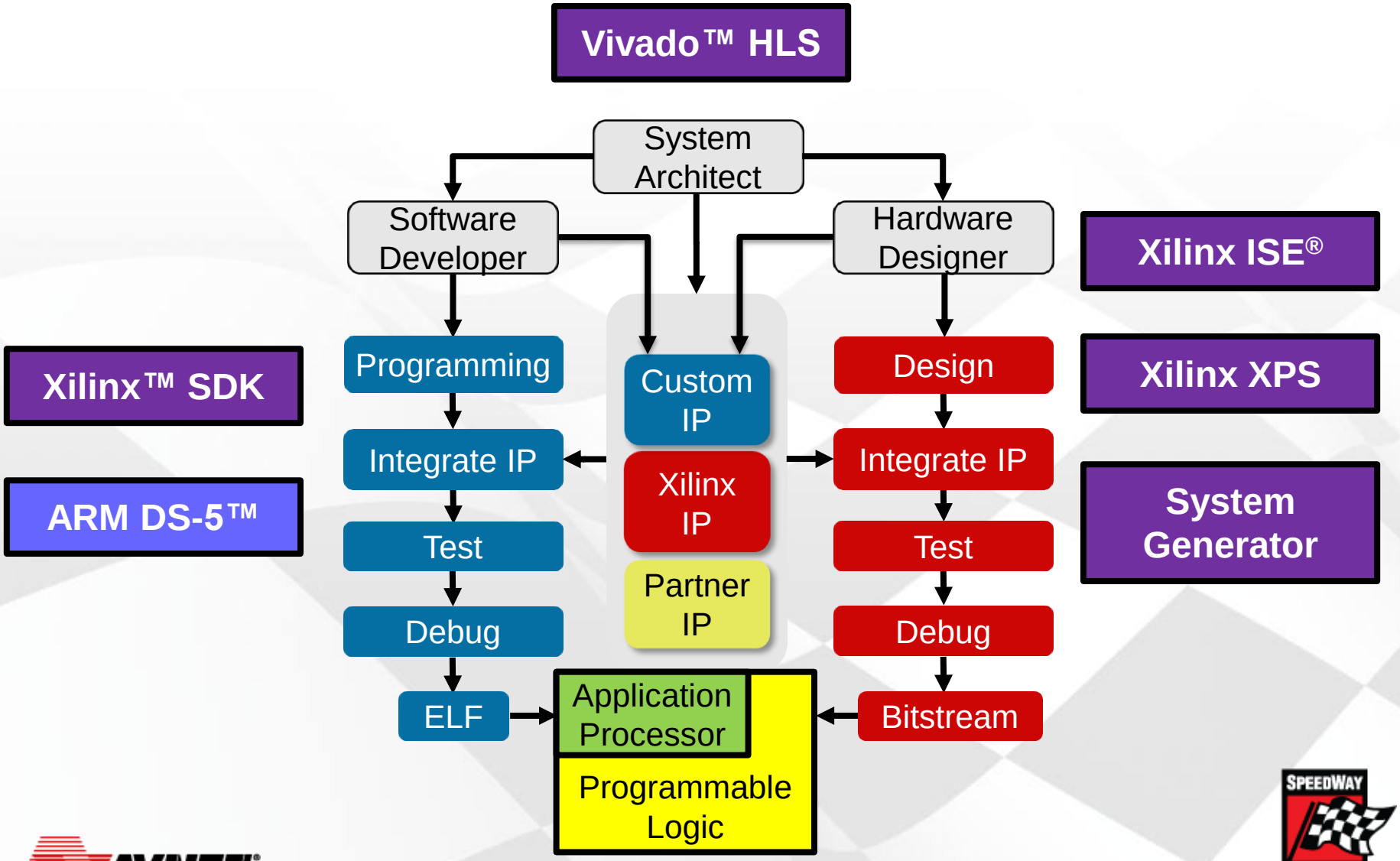
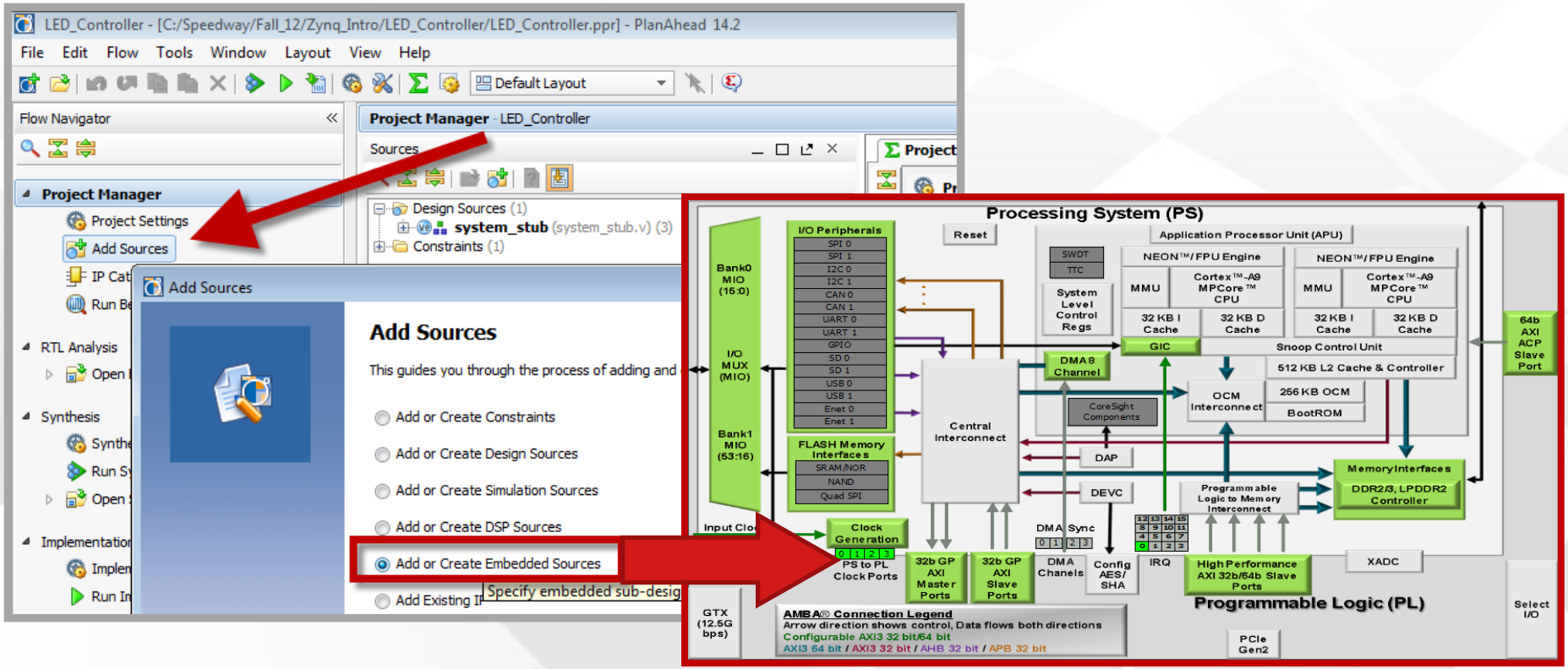
Zynq-7000 AP SoC Embedded Design Flow

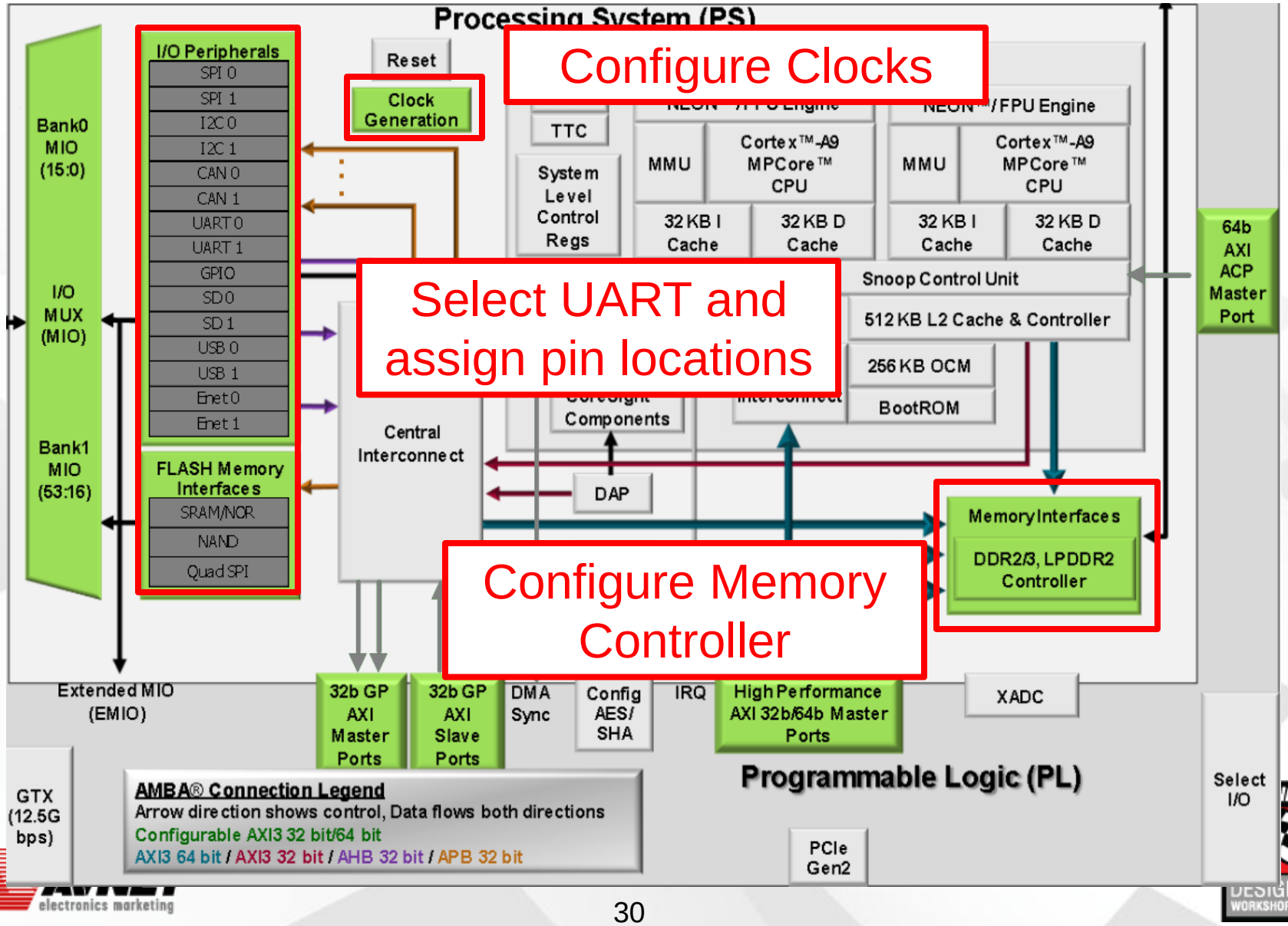


Getting Started: Adding an Embedded Source

1. **Create Embedded Source in PlanAhead**
2. **Customize Zynq Processor in XPS**

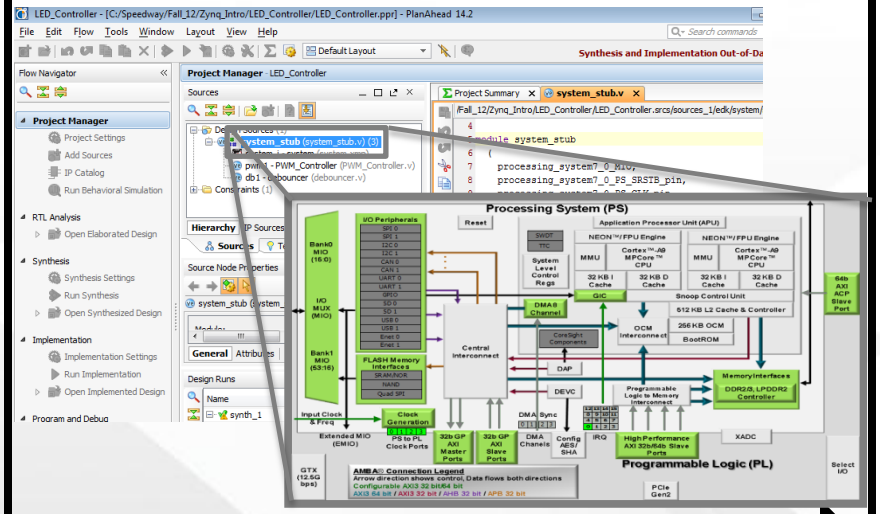


Configure PS



How is XPS Related to SDK?

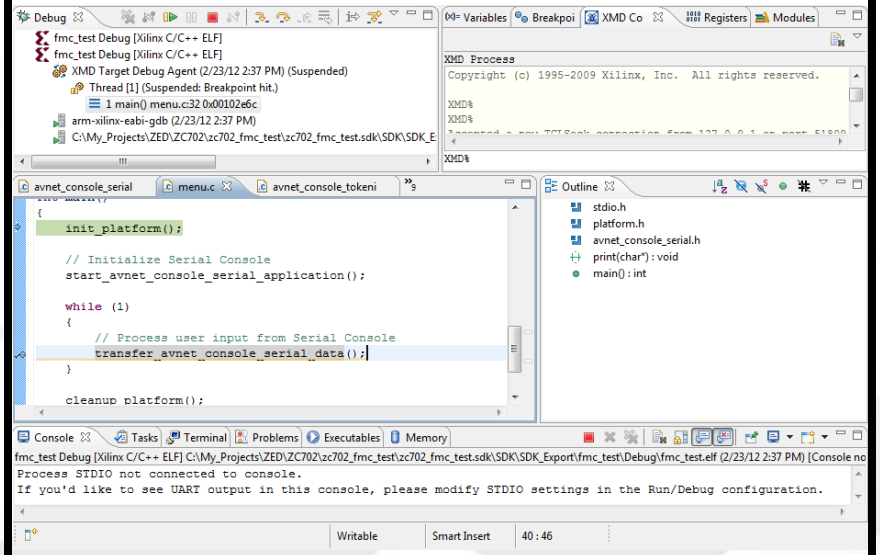
PlanAhead/XPS



Export Hardware Design

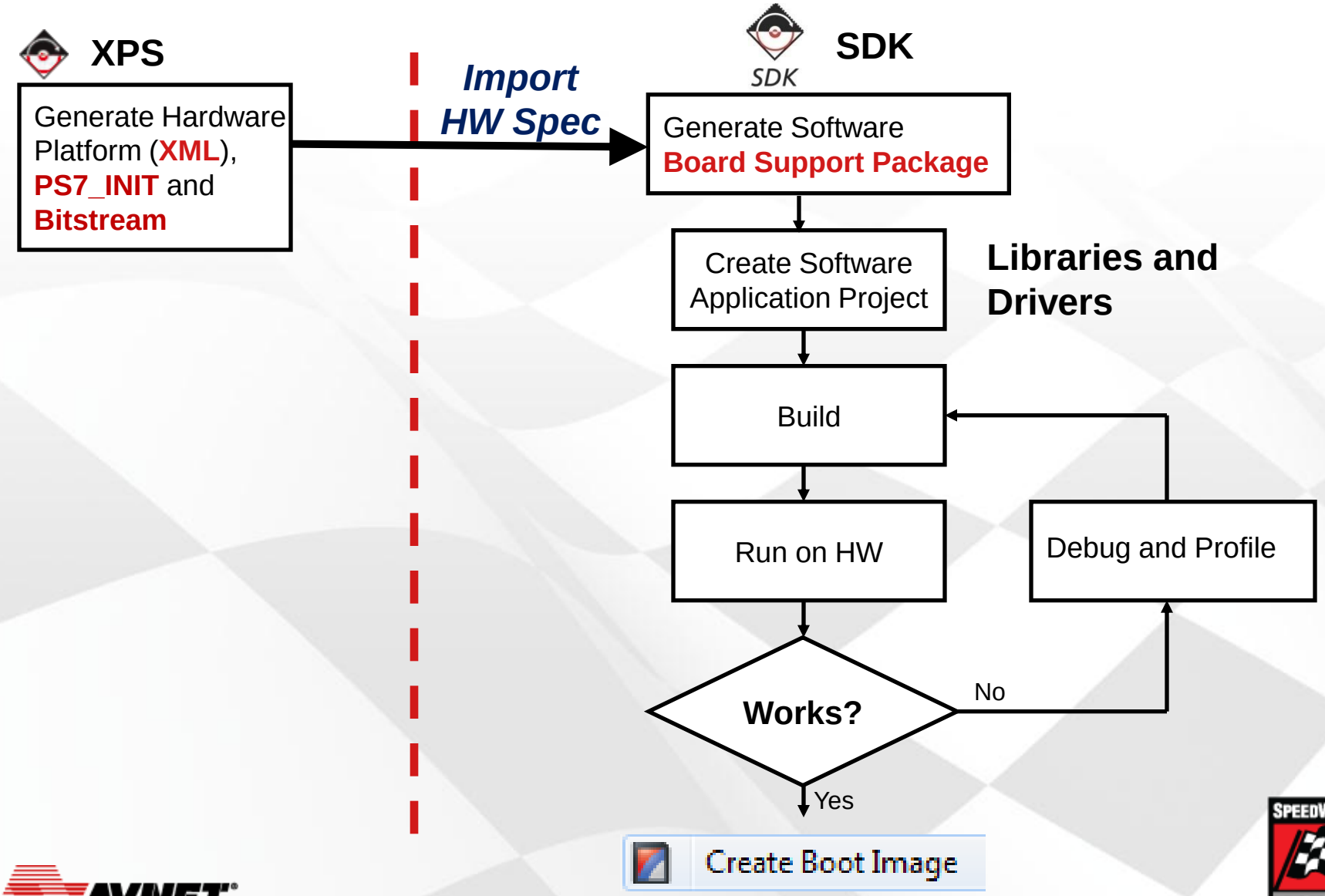
- Define PS Subsystem
- Configure MIO Peripherals
- Connect PL hardware to PS

Software Development Kit



- Build ARM executable and debug directly on target hardware
- Auto-generate BSP, FSBL targeted to hardware

SDK Application Development Flow



Software Development Tools

Xilinx Supplied

ARM Supplied

3rd Party Supplied

	Xilinx Basic Features	ARM® Fully Featured	3rd Party Cortex™A9 Vendors
Software Platform	Standalone and Linux Drivers Example Boot Code	Drives Connected Community	Operating Systems Middleware Codecs, etc.
Software Development	Platform Studio SDK (Eclipse IDE) ARM GNU CC	ARM® Development Studio IDE (DS-5)	IDEs, OS-specific
Debug	Platform Studio SDK SDK Profiler	DS-5 Debugger / Profiler	Debuggers & Profilers
	USB Cable download, run-time control	RVI Debug DSTREAM Trace	ICE & Trace
	JTAG / ARM CoreSight™ Infrastructure		

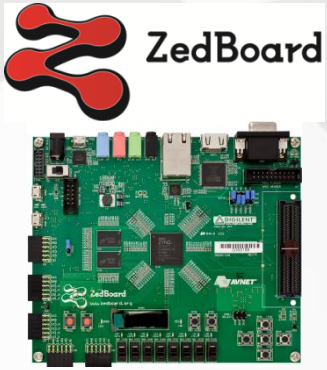
Course Objectives

- Embedded Processor Challenge
- Zynq-7000 AP SoC Family Overview
- Zynq-7000 AP SoC Ecosystem
- Zynq-7000 AP SoC HW & SW Design Tools and Flow
- **Zynq-7000 AP SoC Development Kits, Training, and Reources**

Zynq-7000 Development Kits

- **Learn more about the Zynq-7000 AP SoC**
  - Visit www.xilinx.com/zynq
- **Purchase a Zynq development kit**

ZedBoard
www.zedboard.org
P/N: AES-Z7EV-7Z020-G
Price: $395
Available: July 2012



ZC702 Evaluation Kit
www.xilinx.com/zc702
P/N: EK-Z7-ZC702-CES-G
Price: $895
Available: June 2012

Zynq Video & Imaging Kit
www.xilinx.com/products/boards-and-kits/DK-Z7-VIDEO-G.htm
P/N: EK-Z7-VIDEO-CES-G
Price: $1495
Available: June 2012

Where to get more trainings

Xilinx Authorized Training Partner (ATP) Courses

- **Accelerating Design Productivity with SDK**
  - Processors, Peripherals, and Tool Utilization
  - Application Profiling Techniques
  - Writing Custom Device Drivers
- **Details of Using Zynq Processor**
  - Advanced Boot Methodologies
  - Cortex-A9 Processor Services
  - Advanced DMA Controller

Embedded Systems Software Design (2 Days, Level 3)
www.xilinx.com/training/atp.htm

Advanced Features and Techniques of Embedded Systems Software Design (1 Day, Level 4)
www.xilinx.com/training/atp.htm

Online Resources

- Xilinx Zynq Linux Wiki
  wiki.xilinx.com/zynq-linux
- Xilinx Design Tools
  www.xilinx.com/products/design-tools/index.htm
- ZedBoard Community (tutorials, forums)
  www.zedboard.org
- Avnet Online OnDemand Trainings
  www.zedboard.org

AVNET electronics marketing

SPEEDWAY DESIGN WORKSHOPS

Thank you.