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SMPTE 2022-5/6 High Bit Rate Media Transport Over IP Networks with Forward Error Correction

Author: Gilbert Magnaye, Josh Poh, Myo Tun Aung and Tom Sun

Summary

This application note covers the design considerations of a Video Over IP networks system using the performance features of the LogiCORE™ IP SMPTE 2022-5/6 Video Over IP transmitter and receiver cores. The design focuses on high bit rate, native media transport over 10 Gb/s Ethernet with a built-in forward error correction (FEC) engine. The design is able to support up to three SD/HD/3G-SDI streams.

The reference design has two platforms: the transmitter platform and the receiver platform. The transmitter platform design uses three SMPTE SDI cores to receive the incoming SDI video streams. The received SDI streams are multiplexed and encapsulated into fixed-size datagram packets by the SMPTE 2022-5/6 Video Over IP transmitter core and sent using the 10-Gigabit Ethernet MAC core. The ten gigabit link is supported by a 10-Gigabit Ethernet PCS/PMA core using an optical cable connected to the receiver end. On the receiver platform, the Ethernet datagram packets are collected at the 10-Gigabit Ethernet MAC. The SMPTE 2022-5/6 Video Over IP receiver core filters the datagram packets, de-encapsulates and de-multiplexes the datagrams into individual streams which are output through the SMPTE SDI cores. The Ethernet datagram packets are buffered in DDR3 SDRAM for both the transmitter and receiver. The DDR traffic passes through the AXI4 interconnect to the 7 series AXI memory controller. A MicroBlaze™ processor is included in the design to initialize the cores and read the status.

The reference design targets the Xilinx Kintex®-7 FPGA KC705 evaluation kit [Ref 1], which uses the Kintex-7 XC7K325T-2FFG900 FPGA and the Inrevium TB-FMCH-3GSDI2A [Ref 2] mezzanine card.

Included Systems

The reference design was created and built using the Vivado® Design Suite, System Edition 2013.4. The design also includes software built using the Xilinx Software Development Kit (SDK) 2013.4. The software runs on the MicroBlaze processor subsystem and implements control and status functions. Complete project files for Vivado Design Suite and the SDK are provided with this application note to allow examination and rebuilding of the design or to use it as a template for starting a new design. See Reference Design.

Introduction

This application note permits the demonstration of SMPTE2022-5/6 standard video streams transmitted over a 10 Gb/s Ethernet network using a provided reference design incorporating readily-available Xilinx IP cores and hardware evaluation kits. The reference design is built around the SMPTE 2022-5/6 Video Over IP transmitter and receiver cores and leverages additional Xilinx IP cores to form the complete system. The input and output of the system are SDI video streams. The system consists of two platforms. The transmitter and receiver cores each reside in separate platforms. An optical cable connects the two platforms simulating an IP network. See Figure 1.

The SMPTE SDI core allows the video over IP cores to receive and transmit SDI streams while the 10-Gigabit Ethernet MAC and 10-Gigabit Ethernet PCS/PMA enable the video over IP cores to transfer SDI data in the Ethernet medium. See Figure 2 and Figure 3.

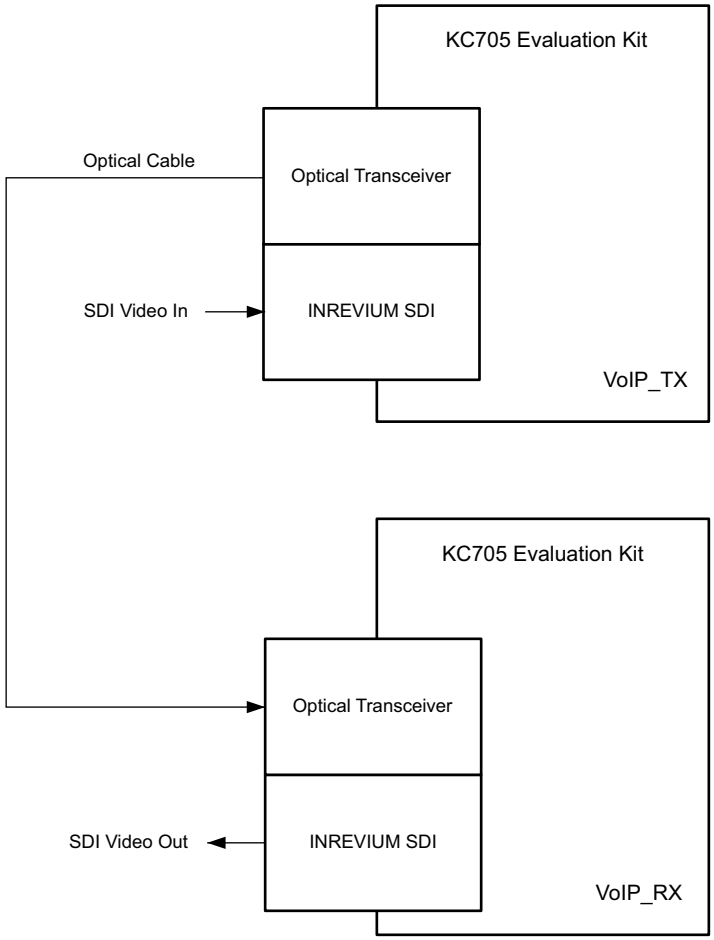

Figure 1: **Top-Level Video Over IP System on KC705 Evaluation Board**

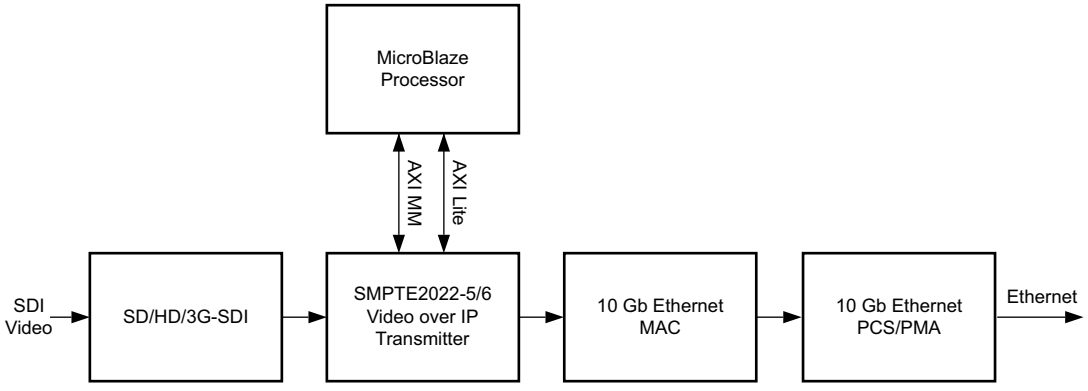

Figure 2: **Transmit Platform Diagram**

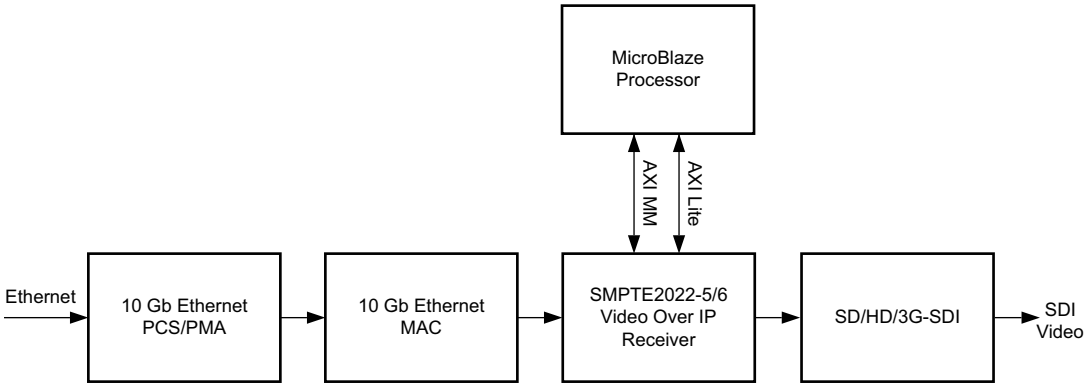

Figure 3: **Receive Platform Diagram**

As well as managing the encapsulation and de-encapsulation of the SDI streams, the transmitter and receiver cores include FEC protection features. FEC protects the video stream during the transport of high-quality video over IP networks. With FEC, the transmitter adds systematically generated redundant data to its video. This redundancy allows the receiver to detect and correct a limited number of packet errors occurring anywhere in the video without the need to query the transmitter for additional video data. These errors, in the form of lost video packets, result from several causes ranging from thermal noise to storage system defects and transmission noise introduced by the environment. FEC gives the receiver the ability to correct these errors without needing a reverse channel to request retransmission of data. This feature can be enabled using the core registers.

High-level control of the system is provided by a simplified MicroBlaze embedded processor subsystem containing I/O peripherals and processor support IP cores. A clock generator block and a processor system reset block supply clock and reset signals for the system, respectively. An AXI4 interconnect and an AXI4 memory interface generator (MIG) are instantiated in the subsystem allowing the video over IP cores access to the DDR3 SDRAM. See Figure 4 and Table 1 for a block diagram of the MicroBlaze processor subsystem and its address map.

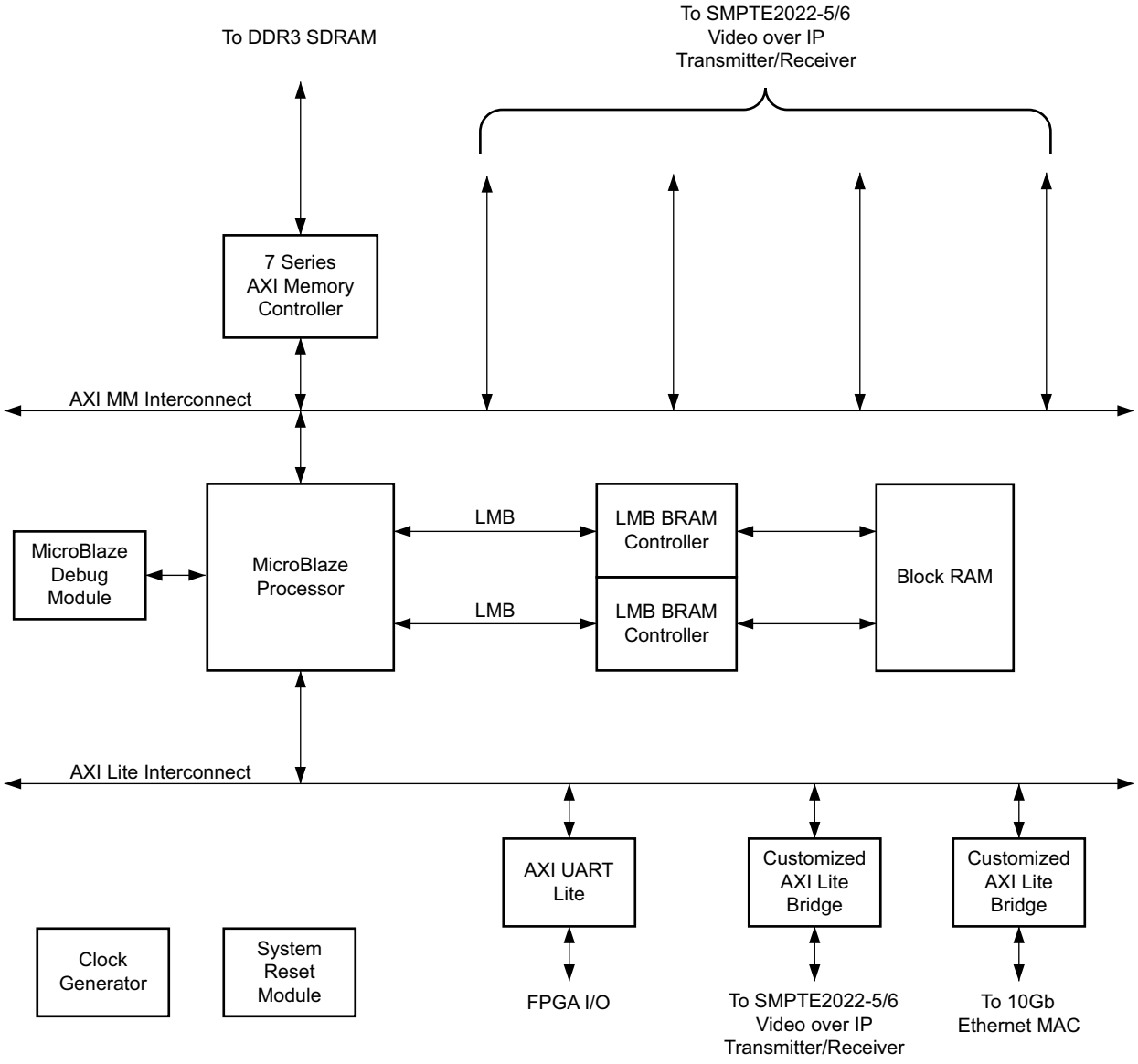

Figure 4: **MicroBlaze Processor System Block Diagram**

Table 1: **MicroBlaze Processor Subsystem Address Map**

Peripheral	Instance	Base Address	High Address
lmb_bram_if_cntlr	ilmb_bram_if_cntlr	0x00000000	0x0001ffff
lmb_bram_if_cntlr	dlmb_bram_if_cntlr	0x00000000	0x0001ffff
mig_7series	mig_1	0xc0000000	0xffffffff
axi_uartlite	axi_uartlite_1	0x40600000	0x4060ffff
axilite_bridge	smpte2022_axilite	0x70e00000	0x70e0ffff
axilite_bridge	ten_gig_eth_mac_axilite	0x7c400000	0x7c400FFF

Hardware Requirements

The hardware requirements for the reference design are:

- Two Xilinx Kintex-7 FPGA KC705 Evaluation Kit boards
- Two Inrevium 3G-SDI Boards (TB-FMCH-3GSDI2A)
- Two SFP+ Optical Transceiver modules
- Optical Cable
- Vivado Design Suite 2013.4
- SDK 2013.4

Reference Design Specifics

Other than the SMPTE 2022-5/6 Video Over IP transmitter and receiver cores, the reference design includes these cores:

- AXI Interconnect
- MicroBlaze Processor
- MicroBlaze Processor Debug Module
- Local Memory Bus
- LMB Block RAM Interface Controller
- Block Memory Generator
- Clocking Wizard
- Processor System Reset Module
- AXI UART Lite
- SMPTE2022 AXI4-Lite Bridge (customized)
- MIG 7 Series
- SMPTE SD/HD/3G-SDI
- 10-Gigabit Ethernet MAC
- 10-Gigabit Ethernet PCS/PMA

Hardware System Specifics

This section describes the high-level features of the reference design, including how the main IP blocks are configured.

Video Over IP System

The reference design implements the SMPTE 2022-5/6 Video Over IP cores as modules for broadcast applications that require bridging between broadcast connectivity standards (SD/HD/3G-SDI) and a 10 Gb/s Ethernet network. The cores are intended for developing Internet protocol-based systems to reduce the overall cost in broadcast facilities for distribution and routing of audio and video data. The SDI data to be transported are mapped into media datagram payloads as per SMPTE 2022-6. The systematically-generated redundant forward error correction datagram packets are formatted according to SMPTE 2022-5. IP/UDP/RTP protocols provide standard headers when transporting the media and FEC datagram packets over the IP network.

To support the system functions correctly, the bandwidth available in the network must meet or exceed what is required to support the stream generated by the system. The overhead required for media datagram generation is approximately 5% due to the IP/UDP/RTP and SMPTE 2022-6 headers.

SMPTE 2022-5/6 Video Over IP Transmitter

The SMPTE 2022-5/6 Video Over IP transmitter in the reference design is configured to accept three channels of SDI input from the SMPTE SDI receiver. The transmitter connects to the 10-Gigabit Ethernet MAC through an AXI4-Stream data interface. The transmitter also connects to a customized IP core in the MicroBlaze processor subsystem through an AXI4-Lite control interface. The transmitter core does not have native EDK support, hence a customized IP core called `axilite_bridge` is created for register access. The transmitter core uses two AXI4 external master connectors to access the DDR3 SDRAM through the AXI4 interconnect. The memory map address range is fixed at `0xC0000000` — `0xFFFFFFFF`.

The transmitter source MAC address is set to `0x000000000000AA`. The transmitter source IP address is set to 192.168.1.100 and the destination IP address for all channels is set to 192.168.1.50. The UDP ports are configured as shown in Table 2. The FEC matrix sizes set for the channels are shown in Table 3. These parameters are configurable through the registers.

Table 2: **UDP Port Values for SDI Channels**

BNC connector	Channel	Source UDP port	Destination UDP port
RX1	0	`0x10`	`0x10`
RX2	1	`0x20`	`0x20`
RX3	2	`0x30`	`0x30`

Table 3: **FEC Matrix Size Values for SDI Channels**

BNC connector	Channel	L	D
RX1	0	77	77
RX2	1	77	77
RX3	2	77	77

The SMPTE 2022-5/6 Video Over IP transmitter contains an AXI4-Lite interface which allows dynamic control of the parameters within the core from a processor. For more information about the registers, see the *LogiCORE IP SMPTE 2022-5/6 Video over IP Transmitter Product Guide* (PG032) [Ref 4].

The registers are divided into two categories: general space registers and channel space registers. The parameters in the general space registers apply to all channels. The parameters in the channel space registers apply to each individual channel.

For the general space registers, normal address read and write access is applied. For the Channel space registers, follow these steps to update the registers:

1. Set the channel to configure at register address `base_addr+0x030`.
2. Configure the channel-specific register.
3. Pulse the `reg_update` bit of the Control register to commit the change to the channel register.
4. Repeat step 1 through step 3 for each additional channel or register. See Figure 5.

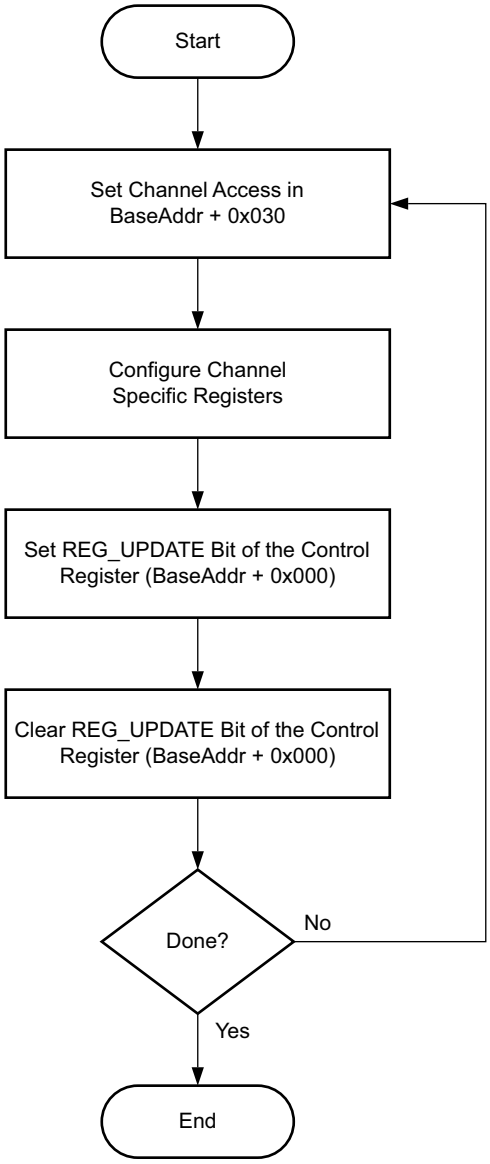

Figure 5: **Channel Register Configuration Flow Chart**

SMPTE 2022-5/6 Video Over IP Receiver

The SMPTE 2022-5/6 Video Over IP receiver in the reference design is configured to stream three channels of SDI output to the SMPTE SDI transmitters. The receiver connects to the 10-Gigabit Ethernet MAC through an AXI4-Stream data interface. The receiver also connects to a customized IP core in the MicroBlaze processor subsystem through an AXI4-Lite control interface. The receiver core does not have native EDK support, hence a customized IP core called `axilite_bridge` is created for register access. The receiver core uses three AXI4 external master connectors to access the DDR3 SDRAM through an AXI4 interconnect. The memory map address range is fixed at `0xC0000000` — `0xFFFFFFFF`. The SMPTE 2022-5/6 Video Over IP receiver uses a VCXO replacement solution for video clock recovery. See the *All Digital VCXO Replacement for Gigabit Transceiver Applications Application Note* (XAPP589) [Ref 11] for details.

The incoming media packets are filtered based on the IP source address, SSRC and UDP destination ports shown in Table 4.

Table 4: **UDP Port Values for SDI Channels**

BNC connector	Channel	Destination UDP port
TX1	0	0x10
TX2	1	0x20
TX3	2	0x30

The media packets per channel to be buffered prior to starting the SDI output is set at 14,000.

The SMPTE 2022-5/6 Video Over IP receiver contains an AXI4-Lite interface which allows dynamic control of the parameters within the core from a processor. For more information about the registers, see the *LogiCORE IP SMPTE 2022-5/6 Video over IP Receiver Product Guide* (PG033) [Ref 5].

The registers are divided into two categories: general space registers and channel space registers. The parameters in the general space registers apply to all channels. The parameters in the channel space registers apply to each individual channel.

For the general space registers, normal address read and write access is applied. For the Channel space registers, follow these steps to update the registers:

1. Set the channel to configure at register address `base_addr+0x030`.
2. Configure all channel registers of interest for the particular channel.
3. Pulse the `reg_update` bit of the Control register to commit changes to the channel registers.
4. Repeat step 1 through step 3 for each additional channel. See Figure 5, page 7.

SMPTE SD/HD/3G-SDI

The SMPTE SDI core provides transmitter and receiver interfaces for SMPTE SD-SDI, HD-SDI and 3G-SDI standards. The core is connected to 7 series FPGA GTX transceivers to serialize and deserialize the SDI video streams. The SMPTE SDI receiver uses a 148.5 MHz GTX transceiver reference clock frequency to receive its supported SDI bit rates. The receiver automatically determines the incoming SDI bit rate and configures itself and the GTX transceiver appropriately for that SDI mode. The SMPTE SDI transmitter requires two different GTX transceiver reference clock frequencies to supply the supported SDI bit rates of 148.5 MHz and 148.35 MHz specified in the design. The clock multiplexer built into the GTX transceiver switches between these two reference clocks. A port dynamically determines the operating SDI mode for the transmitter. The transmitter, in turn, controls the GTX transmitter through the dynamic reconfiguration port (DRP) to provide the appropriate configuration for each SDI mode. See the *SMPTE SD/HD/3G-SDI Product Guide* (PG071) [Ref 6] for more information.

10-Gigabit Ethernet MAC

The AXI4-Stream interface of the transmitter 10-Gigabit Ethernet MAC instance is connected to the output of the SMPTE 2022-5/6 Video Over IP transmitter. The AXI4-Stream interface of the receiver 10-Gigabit Ethernet MAC instance is connected to the input of the SMPTE 2022-5/6 Video Over IP receiver. A 64-bit SDR PHY port is configured in the 10-Gigabit Ethernet MAC to interface to the 10-Gigabit Ethernet PCS/PMA core. No flow control is used. See the *LogiCORE IP 10-Gigabit Ethernet MAC Product Guide* (PG072) [Ref 7] for more information.

10-Gigabit Ethernet PCS/PMA

The 10-Gigabit Ethernet PCS/PMA core creates a 10GBASE-R optical link between the video over IP transmitter and receiver platforms. The PCS/PMA uses ones transceiver to achieve a 10 Gb/s data rate. An optical cable is connected between the SFP+ optical transceivers on both

platforms. The PCS/PMA 10GBASE-R/KR standard is fully specified in clauses 45, 49, 72, 73, and 74 of the 10-Gigabit Ethernet IEEE 802.3-2008 specification. See the *LogiCORE IP 10-Gigabit Ethernet PCS/PMA Product Guide* (PG068) [Ref 8] for more information.

AXI Interconnect (AXI_MM)

This AXI4 interconnect instance provides the high F_{MAX} and throughput required by the design with a 256-bit core data width and a 200 MHz clock frequency. The AXI4 interconnect core data width and clock frequency match the capabilities of the attached AXI4 MIG so that width and clock converters are not required. Setting the AXI4 interconnect core data width and clock frequency below the native width and clock frequency of the memory controller creates a bandwidth bottleneck within the system. To help meet the timing requirements of a 256-bit AXI4 interface at 200 MHz, a rank of register slices are enabled between the AXI_MM interconnect and the AXI4 MIG. Together, the AXI4 interconnect and AXI4 MIG form a 4-port AXI4 multi-port memory controller (MPMC) connected to four AXI4 external master connectors. The AXI4 interconnect configuration is consistent with the system performance optimization recommendations for an AXI4 MPMC-based system as described in the *AXI Reference Guide* [Ref 9].

Memory Interface Generator

The Memory Interface Generator forms the single slave connected to the AXI4 Interconnect. The MIG AXI4 interface is 256 bits wide and runs at 200 MHz with disabled narrow burst support for optimal throughput and timing. This configuration matches the native AXI4 interface clock and width corresponding to a 64-bit DDR3 DIMM with an 800 MHz memory clock which is the nominal performance of the memory controller for a Kintex-7 device with a -2 speed grade. Register slices are enabled to ensure that the interface meets timing at 200 MHz. These settings ensure that a high degree of transaction pipelining is active to improve system throughput. See the *7 Series FPGAs Memory Interface Solutions User Guide* (UG586) [Ref 10] for more information.

AXI Interconnect (AXI lite)

The MicroBlaze processor data peripheral (DP) interface master writes and reads control and status information to all AXI4-Lite slave registers in the design. Because these are 32-bit interconnects and do not require high F_{MAX} and throughput, they are connected to a slower F_{MAX} portion of the design by a separate AXI Interconnect. The AXI4-Lite Interconnect block is configured for shared-access mode because of the lower throughput in this portion of the design and to allow area to be optimized over performance on this interconnect block. Also, this interconnect is clocked at 100 MHz to ensure that synchronous integer ratio clock converters in the AXI Interconnect can be used which offer lower latency and less area than asynchronous clock converters. The AXI_Lite Interconnect slaves consist of AXI UART Lite cores and a customized `axilite_bridge` IP core connecting to the 10-Gigabit Ethernet PCS/PMA and SMPTE 2022-5/6 Video Over IP transmitter or receiver cores.

Software Configuration

The software application initializes the video over IP transmitter and receiver platforms. After software initialization, commands can be selected from the menu of the UART terminal display.

Application-level software and the drivers for controlling the system are written in C. Alternatively, drivers and application software can write directly to the IP control registers.

The software configures the register values for the transmitter and receiver. The transmitter general space register values are shown in Table 5 and the channel space register values are shown in Table 6. The receiver general space register values are shown in Table 7 and the channel space register values are shown in Table 8. The base address of the register set is the AXI4-Lite bridge base address (`0x70E00000`). Registers not shown in the tables are not initialized and remain at their respective default values.

Table 5: **Initialized Transmitter General Space Register Values**

Offset	Register Name	Value
0x060	Src_mac_low_addr	0x000000AA
0x064	Src_mac_high_addr	0x00000000
0x068	Src_IP_addr	0xC0A80064

Table 6: **Initialized Transmitter Channel Space Register Values**

Offset	Register Name	Value		
		Channel 1	Channel 2	Channel 3
0x100	chan_en	0x1	0x1	0x1
0x104	FEC_config	0x7	0x7	0x7
0x10C	FEC_L	0x4D	0x4D	0x4D
0x110	FEC_D	0x4D	0x4D	0x4D
0x128	dest_ip_addr	0xC0A80032	0xC0A80032	0xC0A80032
0x138	src_udp_port	0x10	0x20	0x30
0x13C	dest_udp_port	0x10	0x20	0x30
0x140	SSRC	0x12345600	0x12345610	0x12345620
0x144	RTP TOS (2) TTL (64)	0x00020040	0x00020040	0x00020040
0x148	FEC TOS (3) TTL (65)	0x00030041	0x00030041	0x00030041

Table 7: **Initialized Receiver General Space Register Values**

Offset	Register Name	Value
0x060	mac_low_addr	0x000000BB
0x064	mac_high_addr	0x00000000
0x068	IP_host_addr	0xC0A80032

Table 8: **Initialized Receiver Channel Space Register Values**

Offset	Register Name	Value		
		Channel 1	Channel 2	Channel 3
0x100	chan_en	0x1	0x1	0x1
0x110	firewall_sel	0x0	0x0	0x0
0x114	dest_port	0x10	0x20	0x30
0x118	SSRC	0x12345600	0x12345610	0x12345620
0x11C	src_ip_host_addr	0xC0A80064	0xC0A80064	0xC0A80064
0x12C	start_buffer_size	0x36B0	0x36B0	0x36B0

Figure 6 shows the video over IP transmitter and receiver overall software precess.

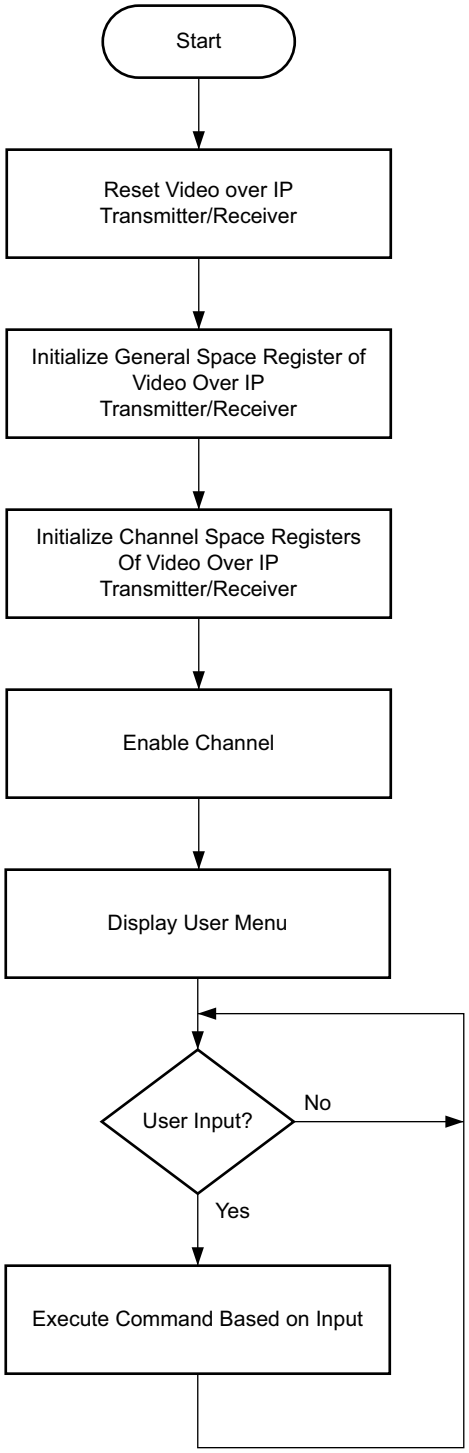

Figure 6: **Video Over IP Transmitter and Receiver Overall Software Process**

Note: Channel enable is asserted last to ensure proper core operation after reset.

It is recommended that the Video Over IP cores be reset during the system setup stage. Instability can result if reset is asserted during operation.

Executing the Reference Design in Hardware

This section provides instructions detailing the setup and operation of the reference design on the KC705 evaluation board using the Inrevium TB-FMCH-3GSDI2A mezzanine boards (Figure 7 and Figure 8).

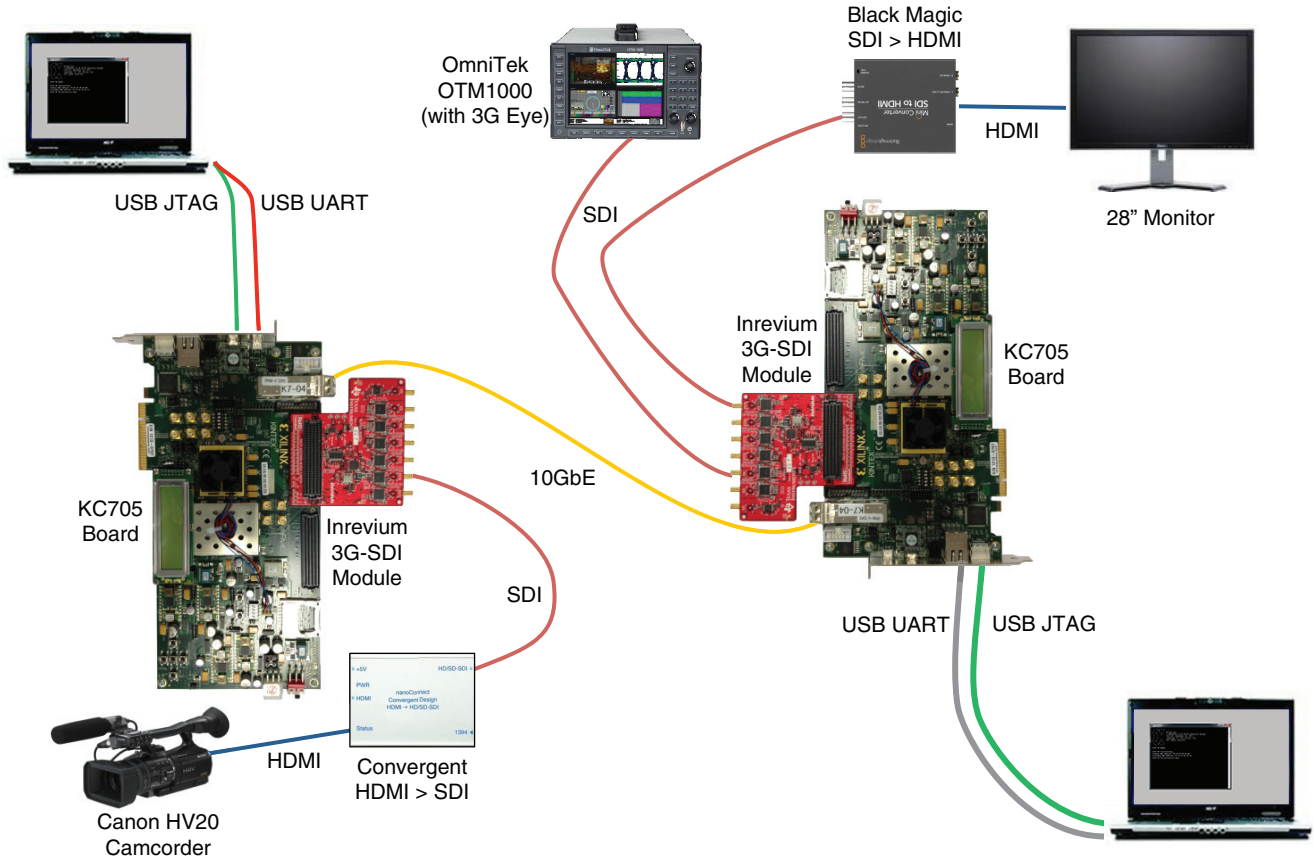

Figure 7: **Video Over IP System**

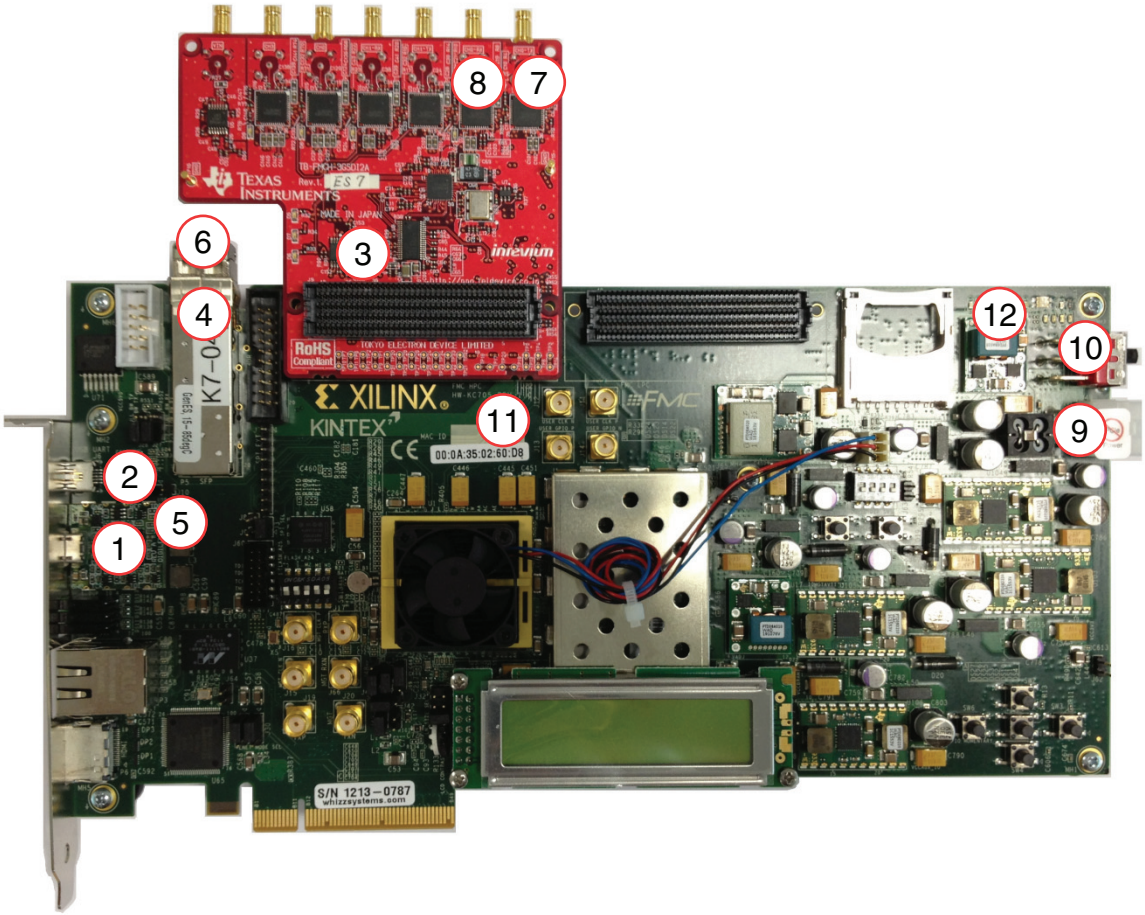

Figure 8: **KC705 and TB-FMCH-3FSDI2A Boards**

In these instructions, numbers in parentheses correspond to callout numbers in Figure 8.

1. Connect a USB cable from the host PC to the USB JTAG port (1). Ensure the appropriate device drivers are installed.
2. Connect a second USB cable from the host PC to the USB UART port (2). Ensure that the USB UART drivers described in the section Hardware Requirements have been installed.
3. Connect a TB-FMCH-3GSDI2A board to the HPC-FMC connector of the KC705 boards (3).
4. Connect an SFP+ optical transceiver module (6) to the SFP connector (4) of the KC705 boards.
5. Connect a jumper to J4 (5) on the KC705 boards to enable the SFP+ transmitter.
6. Connect one end of the optical cable to the SFP+ transceiver module on the video over IP transmitter board (6), and connect the other end to the optical cable to the SFP+ transceiver of the video over IP receiver board.
7. On the video over IP receiver board, connect the SDI video monitor cables to the TB-FMCH-3GSDI2A 3G/HD/SD Channel 0, 1 and 2 DIN connectors (7).
8. On the video over IP transmitter board, connect the SDI video generator cables to the TB-FMCH-3GSDI2A 3G/HD/SD Channel 0, 1 and 2 DIN connectors (8).
9. Connect a power supply to the J49 connector (9) of the KC705 boards.
10. Set the KC705 board power switch (10) to the ON position.

11. Make sure that the HW-KC705 board revision numbers (11) are the same for both the transmit and receive platforms (see note regarding KC705 evaluation boards prior to revision 1.1).
12. Ensure all LEDs (12) are lit (refer to Debug section for details).
13. Start a terminal program (HyperTerminal, for example) on the host PC with these settings:
    - Baud Rate: **115200**
    - Data Bits: **8**
    - Parity: **None**
    - Stop Bits: **1**
    - Flow Control: **None**

Note: KC705 evaluation board revision numbers below 1.1 (1.0 and C, for example) have the 10Gb ETH PCS/PMA MGT P and N pins swapped. This causes optical signal compatibility issues on standard equipment.
Workaround: Tie TXPOLARITY and RXPOLARITY to VCC in this file:

```
ten_gig_eth_pcs_pma_0
   |
   |_ synth
         |
         |_ ten_gig_eth_pcs_pma_0_gtwizard_10gbaser_gt.VHD
```

Executing the Reference System Using the Pre-Built Bitstream and the Compiled Software Application

This section details the steps necessary to execute the system using the files in the `ready_for_download` directory:

1. Launch the Xilinx Microprocessor Debugger by selecting **Start > All Programs > Xilinx Design Tools > Vivado 2013.4 > SDK**.
2. In the Xilinx command shell window, change to the `ready_for_download` directory:

   VoIP_TX:
   `>cd <unzip_dir>/kc705_smpte2022_56_tx_ip/ready_for_download`

   VoIP_RX:
   `>cd <unzip_dir>/kc705_smpte2022_56_rx_ip/ready_for_download`
3. Download the bitstream to the FPGA:

   `XMD% fpga -f download.bit`
4. Exit the XMD command prompt:

   `XMD% exit`

   Note: The software application starts immediately on completion of FPGA configuration. The executable file (.elf) is embedded in the configuration file (`download.bit`). Start-up order is not critical.

Running the Hardware and Software

Transmitter

A HyperTerminal screen displaying the video over IP transmitter initialization sequence is shown in Figure 9. All three channels are initialized with a different configuration.

```
 ____  ____
 /   /\/   /
/___/  \  /   Xilinx Inc.
\   \   \/    V_SMPTE2022_56_TX 10G
 \   \        Vivado Reference Design
 /   /        Created: November 20, 2013
/___/   /\    Copyright (c) 2013 Xilinx, Inc.
\   \  /  \   All rights reserved.
 \___\/\___\

VoIP TX Reset
VoIP TX Initializing...

Fault Inhibit: Enabled
IP Address:  192.168.0.100
MAC Address: 00-00-00-00-00-AA
Time Stamp:  Enabled
IP Version:  IPv4
VLAN:        Disabled
VLAN Tag:    0xABCD
VoIP TX Initialization done


Initializing Channel 1
Dest IP Addr:  192.168.0.50
Source Port:   0x0010
Dest Port:     0x0010
SSRC:          0x12345600
FEC Size:      77x77
FEC:           On
Block Align:   Block Aligned
FEC TOS:       3
FEC TTL:       65
RTP TOS:       2
RTP TTL:       64
Channel Enabled
Channel 1 Initialization Done

Initializing Channel 2
Dest IP Addr:  192.168.0.50
Source Port:   0x0020
Dest Port:     0x0020
SSRC:          0x12345610
FEC Size:      77x77
FEC:           On
Block Align:   Block Aligned
FEC TOS:       3
FEC TTL:       65
RTP TOS:       2
RTP TTL:       64
Channel Enabled
Channel 2 Initialization Done

Initializing Channel 3
Dest IP Addr:  192.168.0.50
Source Port:   0x0030
Dest Port:     0x0030
SSRC:          0x12345620
FEC Size:      77x77
FEC:           On
Block Align:   Block Aligned
FEC TOS:       3
FEC TTL:       65
RTP TOS:       2
RTP TTL:       64
Channel Enabled
Channel 3 Initialization Done
```

Figure 9: **VOIP_TX Initialization Hyperterminal Output**

Twelve options are displayed on the Main Menu HyperTerminal screen (Figure 10):

1 = Reset Core
2 = Initialize Core (general space registers only)
3 = Change Host IP Address
4 = Change Source MAC Address
5 = Time Stamp Enable/Disable
6 = VLAN Enable/Disable
7 = Change VLAN Tag
8 = 10G MAC Fault Inhibit On/Off (enables single, downstream TX to RX optical link)
c = Configure Channel (opens “Select Channel” submenu)
p = Probe Current Settings (displays status of selected registers in general space)
q = Exit Software Application
? = Display Current Menu

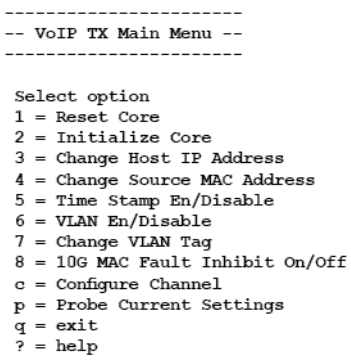

Figure 10: **VOIP_TX Main Menu Hyperterminal Output**

Selecting option **c** produces the Select Channel menu (Figure 11).

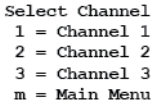

Figure 11: **VOIP_TX Select Channel Menu Hyperterminal Output**

Options allow the choice of one of the three channels or to return to the main menu:

1 = Channel 1
2 = Channel 2
3 = Channel 3
m = Main Menu

After selecting a channel, the Select Option submenu is displayed (Figure 12):

```
Select Option
 1 = Channel Init
 2 = Channel Enable/Disable
 3 = FEC On/Off
 4 = Toggle FEC 1D/2D
 5 = Set Column FEC
 6 = Set Row FEC
 7 = Toggle Block Alignment
 8 = Set Dest MAC Addr
 9 = Set Dest IP Addr
 0 = Set Source UDP Port
 a = Set Dest UDP Port
 b = Set SSRC
 d = Set FEC TOS
 e = Set FEC TTL
 f = Set RTP TOS
 g = Set RTP TTL
 p = Probe Status
 m = Main Menu
 c = Channel Select
```

Figure 12: **VOIP_TX Select Option Submenu Hyperterminal Output**

One of nineteen options in the menu list can be chosen:

1 = Channel Initialization

2 = Channel Enable/Disable

3 = FEC On/Off

4 = Toggle FEC 1D/2D

5 = Set Column FEC

6 = Set Row FEC

7 = Toggle Block Alignment

8 = Set Destination MAC Address

9 = Set Destination IP Address

0 = Set Source UDP Port

a = Set Destination UDP Port

b = Set SSRC

d = Set FEC TOS

e = Set FEC TTL

f = Set RTP TOS

g = Set RTP TTL

p = Probe Status

m = Main Menu

c = Channel Select

Receiver

The video over IP receiver initialization sequence HyperTerminal screen is shown in Figure 13. All three channels are initialized with a different configuration.

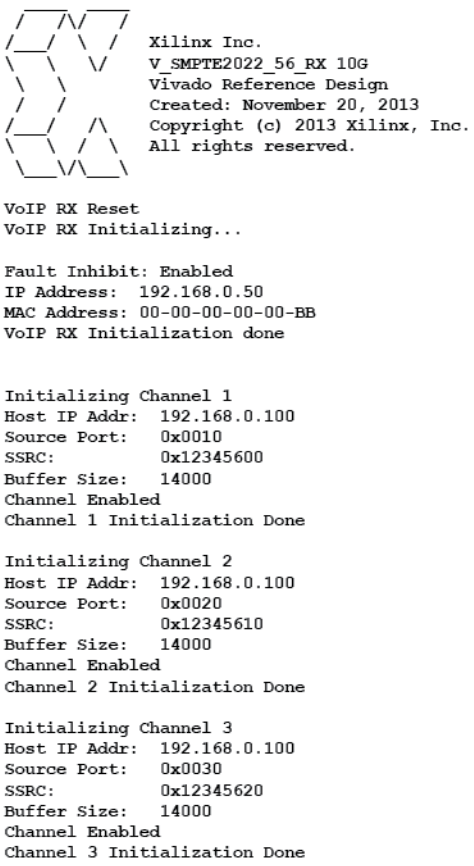

Figure 13: **VOIP_RX Channel Initialization Hyperterminal Output**

Nine options are displayed on the Main Menu HyperTerminal screen (Figure 14):

1 = Reset Core

2 = Initialize Core (general space registers only)

3 = Change Board IP Address

4 = Change MAC Address

5 = 10G MAC Fault Inhibit On/Off (enables single, downstream TX to RX optical link)

c = Configure Channel (opens “Select Channel” submenu)

p = Probe Current Settings (displays status of selected registers in general space)

q = Exit Software Application

? = Display current menu

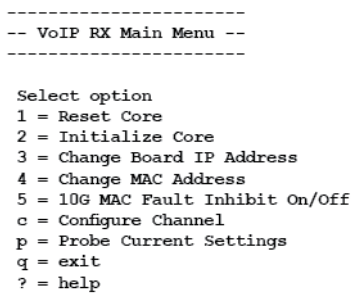

Figure 14: **VOIP_RX Main Menu Hyperterminal Output**

Selecting option **c** produces the Select Channel menu (Figure 15).

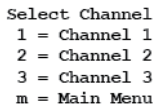

Figure 15: **VOIP_RX Select Channel Menu Hyperterminal Output**

Options allow the choice of one of the three channels or to return to the main menu:

1 = Channel 1

2 = Channel 2

3 = Channel 3

m = Main Menu

After selecting a channel, the Select Option submenu is displayed (Figure 16).

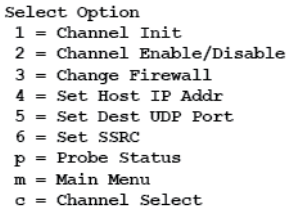

Figure 16: **VOIP_RX Select Option Submenu Hyperterminal Output**

One of nine options in the menu list can be chosen:

1 = Channel Initialization

2 = Channel Enable/Disable

3 = Change Firewall

4 = Set Host IP Address

5 = Set Destination UDP Port

6 = Set SSRC

p = Probe Status

m = Main Menu

c = Channel Select

Rebuilding and Compiling the Reference Design

This section covers rebuilding the hardware design. Before rebuilding the project, ensure that the licenses for the SMPTE 2022-5/6 Video Over IP transmitter and receiver cores, 10-Gigabit Ethernet PCS/PMA and 10-Gigabit Ethernet MAC are installed.

Note: To ensure that no compilation errors occur due to long file paths, unzip the project files as close as possible to the root directory. For example, with a typical Windows installation, unzip the files at C:\.

Generating the Programming File with Vivado Design Suite 2013.4

1. Start Vivado Design Suite
2. At the Tcl Console, change to the workspace directory by typing:

   VoIP_TX:

   ```
   >cd <unzip dir>/kc705_smpte2022_56_tx_ip
   ```

   VoIP_RX:

   ```
   >cd <unzip dir>/kc705_smpte2022_56_rx_ip
   ```

3. To create, compile and generate the project bitstream, run the `all.tcl` script by typing at the Tcl Console:

   ```
   >source all.tcl
   ```

Compiling the Software with SDK

1. After the bitstream generation (all.tcl script) is complete, open the implemented design by clicking **Open Implemented Design** under the Implementation tab on the right.
2. Click **Open Block Design** under the IP integrator tab on the right, then click **system_basic.bd**.
3. At the Sources tab, expand the hierarchy of the project, right-click **i_system_basic** and select **Export Hardware for SDK**.
4. A window appears. Set the workspace and export path to:

   VoIP_TX:
   ```
   <unzip dir>\kc705_smpte2022_56_tx_ip\SW\SDK_Workspace
   ```
   VoIP_RX:
   ```
   <unzip dir>\kc705_smpte2022_56_rx_ip\SW\SDK_Workspace
   ```
5. Ensure that all check boxes are selected and Click **OK**.
6. Import the board support package (BSP) and software applications into the workspace by selecting **File > Import > General > Existing Projects**.
7. Click **Next**, then browse to:

   VoIP_TX:
   ```
   <unzip dir>\kc705_smpte2022_56_tx_ip\SW\SDK_Workspace
   ```
   VoIP_RX:
   ```
   <unzip dir>\kc705_smpte2022_56_rx_ip\SW\SDK_Workspace
   ```
8. Click **OK**.
9. Ensure that all check boxes are selected.
10. Click **Finish**.

The BSP and software applications compile at this step. The process takes 2 to 5 minutes. The existing software applications can now be modified and new software applications can be created in the SDK.

Running the Hardware and Software through the SDK

1. Open the JTAG configuration by selecting **Xilinx Tools > Configure JTAG Settings** (Figure 17).

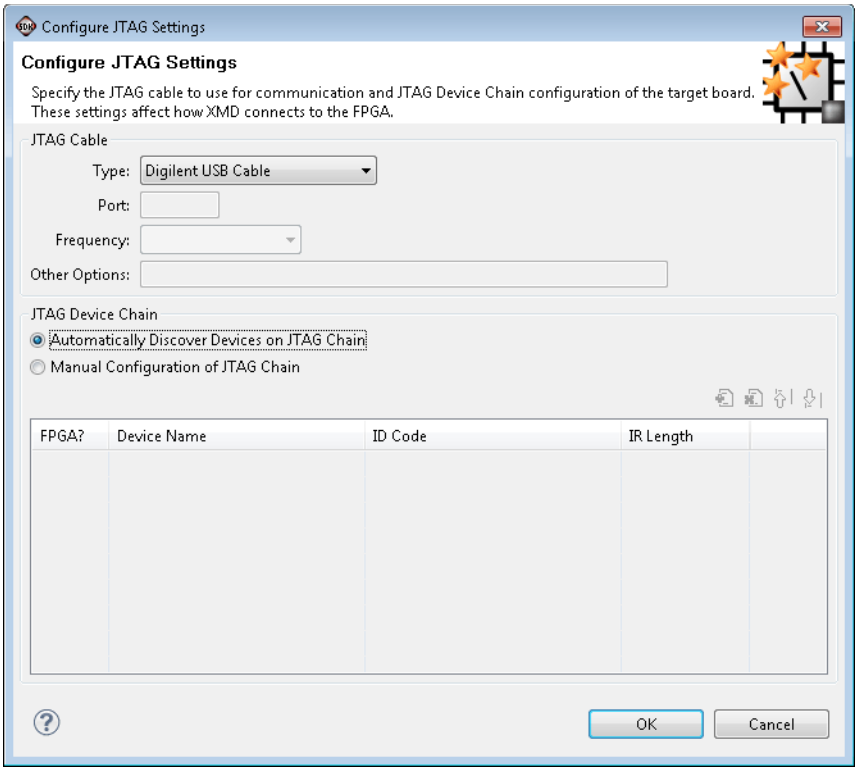

Figure 17: **JTAG Configuration Settings**

2. Select the **Digilent USB Cable** in Type field.
3. Click **Automatically Discover Devices on JTAG Chain**.

   Note: Two workstations are needed when running from the SDK, one for the transmitter and another for the receiver, because the debugger can only connect to one Digilent USB Cable at a time.
4. Click **OK**.
5. Select **Xilinx Tools > Program FPGA**.

   Note: Ensure bootloop is used for `microblaze_0`.
6. Click **Program**.
7. In the Project Explorer window, right-click and select:

   VoIP_TX:
   voip_tx_main > Run As > Launch on Hardware
8. VoIP_RX:
   voip_rx_main > Run As > Launch on Hardware

Note: This reference design does not support Address Resolution Protocol (ARP). Also, the choice is provided whether to run the software application either from MIG or block RAM by editing the linker script. The default setting in the linker script is to execute the software application from block RAM.

The MIG base address in the linker script is set to `0xF8000000` to ensure a generous separation from the memory address range of the video over IP transmitter and receiver cores. For memory requirement details, Refer to *LogiCORE IP SMPTE 2022-5/6 Video over IP Transmitter Product Guide* (PG032) [Ref 4] and *LogiCORE IP SMPTE 2022-5/6 Video over IP Receiver Product Guide* (PG033) [Ref 5].

Additional Information

The `axilite_bridge` custom IP is added as the project local repository during the execution of lines 35-36 of the `proj.TCL` script.

Alternately, the project local repository path can be specified in the Vivado IDE Project Settings dialog box.

Debug

The onboard GPIO LEDs can be used for quick troubleshooting. During normal operation, all LEDs should turn on asynchronously within five seconds after completion of the bitstream configuration. The LED representations are shown in Table 9.

Table 9: **KC705 GPIO LED Designations for Transmitter and Receiver**

GPIO_LED	Designation
0	10G PCS/PMA Link Up
1	10G PCS/PMA Reset Done
2	10G Block Reset (Inverted)
3	10G PCS/PMA 156.25MHz PLL Locked
4	Si5324 Loss-of-Lock (Inverted)
5	Clock 100 MHz Locked
6	Clock 200 MHz Locked
7	DDR Memory Initialization Done

GPIO_LED 0: When Off, this LED can indicate that the opposite platform J4 jumper of is not in place. For example, when VoIP_TX LED 0 is Off, examine the VoIP_RX J4 jumper setting.

GPIO_LED 1 and 2: When Off, these LEDs can indicate that the 156.25MHz clock is missing or not routed to the Ten Gigabit Ethernet MAC and PCS/PMA blocks.

GPIO_LED 3: When Off, this LED can indicate that the differential 156.25MHz reference clock to the 10-Gigabit Ethernet PCS/PMA is missing.

GPIO_LED 7: When Off, this LED indicates that the memory subsystem did not initialize successfully. Try switching the KC705 development boards.

Reference Design

The reference design files for this application note can be downloaded from:

https://secure.xilinx.com/webreg/clickthrough.do?cid=355405, registration required.

Table 10 shows the reference design checklist.

Table 10: **Reference Design Checklist**

Parameter	Description
General	
Developer name	Gilbert Magnaye, Josh Poh, Myo Tun Aung, Tom Sun
Target devices (stepping level, ES, production, speed grades)	Kintex-7 XC7K325T-2FFG900
Source code provided	Yes
Source code format	VHDL (some sources encrypted)
Design uses code/IP from existing Xilinx application note/reference designs, CORE Generator™ software, or third party	Cores generated from Vivado IP catalog

Table 10: **Reference Design Checklist *(Cont'd)***

Parameter	Description
Simulation	
Functional simulation performed	N/A
Timing simulation performed	N/A
Test bench used for functional and timing simulations	N/A
Test bench format	N/A
Simulator software/version used	N/A
SPICE/IBIS simulations	N/A
Implementation	
Synthesis software tools/version used	Vivado 2013.4
Implementation software tools/versions used	Vivado 2013.4
Static timing analysis performed	Yes
Hardware Verification	
Hardware verified	Yes
Hardware platform used for verification	Kintex-7 FPGA KC705 evaluation kit

Design Characteristics

The reference design is implemented using Vivado Design Suite 2013.4 and a Kintex-7 FPGA (XC7K325T-2FFG900) target device.

Utilization and Performance

Table 11 shows the resource utilization for the video over IP transmitter reference design.

Table 11: **Video Over IP Transmitter Resource Utilization**

Resource	Utilization	Available	Percent Utilization
FF	52,197	407,600	13
LUT	45,430	203,800	22
Memory LUT	3,722	64,000	6
I/O	162	500	32
BRAM	170	445	38
DSP48	3	840	1
BUFG	12	32	38
MMCM	2	10	20
PLL	1	10	10
GT	6	20	30

Table 12 shows the resource utilization for the video over IP receiver reference design.

Table 12: **Video Over IP Receiver Resource Utilization**

Resource	Utilization	Available	Percent Utilization
FF	55377	407600	13
LUT	45472	203800	22
Memory LUT	3905	64000	6
I/O	162	500	32
BRAM	195	445	44
DSP48	3	840	1
BUFG	12	32	38
MMCM	2	10	20
PLL	1	10	10
GT	7	20	35

Note: Device resource utilization results depend on the implementation tool versions. Exact results can vary. These numbers should be used as a guideline.

Conclusion

This application note describes a video over IP network system using various Xilinx IP cores. The reference design demonstrates the ability of the SMPTE 2022-5/6 Video Over IP cores to encapsulate and de-encapsulate multiple transport streams into and through a 10 Gb/s Ethernet pipe. The utilization of the Ethernet bandwidth is over 90% with three 3G-SDI streams. The reference design can perform recovery of a limited number of Ethernet packets when impairment is introduced into the network with the forward error correction engine active.

References

This application note uses these references:

1. Kintex-7 FPGA KC705 Evaluation Kit product page
2. Inrevium TB-FMCH-3GSDI2A 3G/HD/SD 3GSDI FMC Connectivity mezzanine card product page
3. AMBA AXI4 specifications
4. *LogiCORE IP SMPTE 2022-5/6 Video over IP Transmitter Product Guide* (PG032)
5. *LogiCORE IP SMPTE 2022-5/6 Video over IP Receiver Product Guide* (PG033)
6. *SMPTE SD/HD/3G-SDI Product Guide* (PG071)
7. *LogiCORE IP 10-Gigabit Ethernet MAC Product Guide* (PG072)
8. *LogiCORE IP 10-Gigabit Ethernet PCS/PMA Product Guide* (PG068)
9. *AXI Reference Guide* (UG761)
10. *7 Series FPGAs Memory Interface Solutions User Guide* (UG586)
11. *All Digital VCXO Replacement for Gigabit Transceiver Applications Application Note* (XAPP589)

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
01/28/2014	1.0	Initial Xilinx release.

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