



XAPP1202 (v1.0) February 26, 2014

# System Traffic Generation and Performance Measurement

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## Summary

This application note demonstrates the AXI4 system traffic generation and system performance measurement using the Xilinx AXI Traffic Generator (ATG) and AXI Performance Monitor (APM) cores. This reference design focuses on run time configuration for different instances of ATG and APM and shows how these IP cores can be configured and programmed to get the system performance metrics. This reference design also shows the run time system throughput and latency of the system for different configuration using web server application.

## Included Systems

The reference design is created and built using Vivado® IP integrator, 2013.4 which is part of Vivado Design Suite: System Editions. The IP integrator is an interactive design and verification environment enabling creation and verification of a hierarchical system by graphically connecting IP provided by Xilinx, third parties, or proprietary IP using interface level connections. It provides a device and platform aware, interactive environment that supports intelligent auto-connection of key IP interfaces, one-click IP subsystem generation, real-time DRCs, and interface change propagation, combined with a powerful debug.

This design also includes the software built using the Xilinx Software Development Kit (SDK). The software runs on MicroBlaze™ processor subsystem and implements control, status, and monitoring functions. The software application is ported on the Xilkernel operating system with web server application. Complete IP integrator and SDK project files are provided with this reference design to allow you to examine and rebuild the design or use it as a template for starting a new design.

## Introduction

Designing the right architecture for a complex and sophisticated FPGA system is a challenging task. The most critical element for meeting the performance requirements of the entire system is the interconnect and memory architecture. These system infrastructure IP components are highly configurable and need to be customized to the communication needs of all the other modules in the system, such as the processor, the graphics unit, and all the external connectivity IP.

Finding the right configuration of the interconnect and memory IP to balance performance requirements and resource considerations requires IP cores which can be used in accurate investigation of architectural trade-offs. Xilinx provides the AXI Traffic Generator and AXI Performance Monitor IP cores which helps you on system performance analysis for Interconnect, memory systems.

The AXI4 Traffic Generator IP is a synthesizable core with various configuration options to generate a wide variety of AXI4/AXI4-Stream and AXI4-Lite traffic. The AXI4 Performance Monitor IP allows you to monitor different AXI4 interfaces in system to get metrics for bytes count, transaction count, latencies, idle cycles, etc. Together these powerful IP features allow you to get a detailed estimation and analysis of the system behavior before the actual IP is ready.

## Hardware and Software Requirements

Hardware requirement for this reference system includes:

- Xilinx KC705 evaluation board (Revision 1.1)
- USB Type-A to Mini-B cable
- USB Type-A to Micro-B cable
- Ethernet CAT-5 cable for connection between Kintex-7 Ethernet port and host system

The installed software tool requirement for building and downloading this reference system includes:

- Vivado Design Suite 2013.4: System Edition
- Vivado SDK 2013.4

## Reference Design Specifics

This application note demonstrates three major system performance modes.

*Table 1: System Performance Modes*

Mode	Description
Memory Performance	This mode demonstrates the memory bandwidth utilization variation for different configuration of seven ATGs used in the subsystem. The seven ATGs configured in static mode with different lengths to stress the interconnect. APMs are used to monitor throughput generated on each ATG memory mapped interface, measure latencies, and utilization on DDR.
High Level Traffic Profile	This mode demonstrates the AXI4 traffic generation for different protocols. The four ATGs configured to mimic AXI4 traffic generated from IP cores like Ethernet, PCIe, Video, and USB. APM monitors throughput generated by each ATG for the above protocol. It also measures latencies and utilization on DDR.
Advanced and Stream	The Advanced mode demonstrates how ATG can be configured to generate fine grained required AXI4 traffic profile by programming ATG commands. This mode also demonstrates the AXI4-Stream traffic generation in the system. APMs monitor throughput generated by each ATG. It also measures latencies and utilization on DDR.

For more detailed information on the ATG and APM, see the product guides in [References, page 21](#).

# System Design

Figure 1 shows the top-level system diagram.

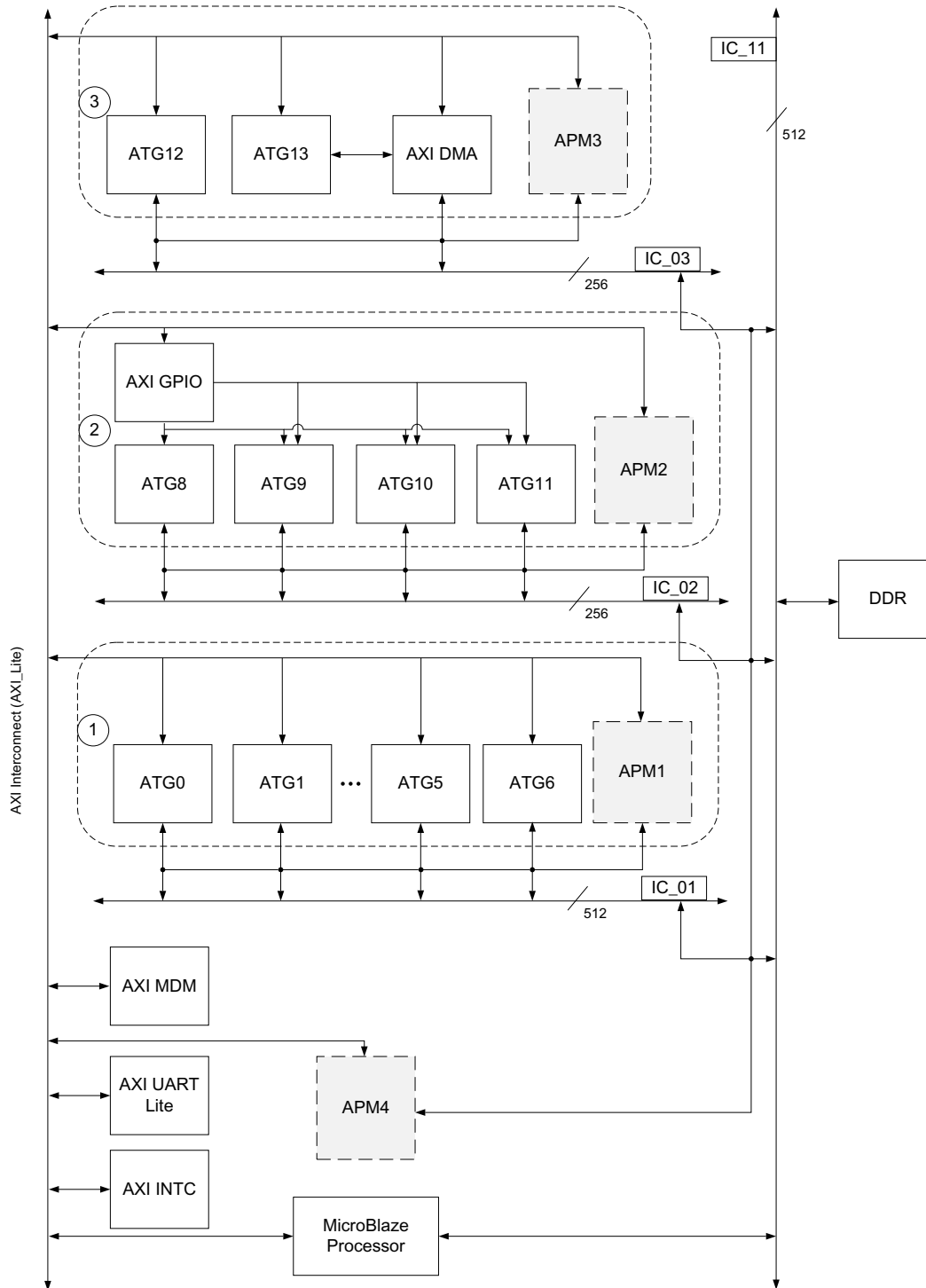


Figure 1: ATG and APM Top-Level System Diagram

At a time, one of the subsystems is active and generates traffic to and from DDR.

- **Subsystem 1** – Memory Performance Mode
- **Subsystem 2** – High Level Traffic Profile Mode
- **Subsystem 3** – Advanced and Streaming Mode

## Memory Performance Mode

This subsystem consists of seven ATGs configured to generate read and write transactions to DDR with burst lengths programmed in each ATG. Together all these ATGs stress the interconnect. APM1 slots connected to each ATG AXI4 port monitors for read and write channel throughput. APM4 monitors the DDR side throughput, utilization, and latency. This mode demonstrates the throughput variation for different master burst length at each ATG and DDR interface.

The software application plots the run time graph for system throughput variation using the web server application. Software application also allows you to change the transfer burst length at each ATG through UART-based user interface and allows you to control the demonstration. This mode gives information about the minimum burst length required for maximum system throughput.

## High Level Traffic Profile Mode

This subsystem consists of four ATGs configured to generate AXI4 traffic similar to real world IP cores such as Ethernet, USB, Video, and PCIe cores. This mode demonstrates the equivalent AXI4 traffic generated for each IP as per the configuration. All of the ATGs start generating traffic on `core_ext_start` pulse generated by using the software application. This allows you to synchronize all of the ATGs. The AXI4 traffic on the ATG can be stopped by providing a `core_ext_stop` pulse.

The following figures show the configuration of each ATG in a High Level Traffic subsystem.

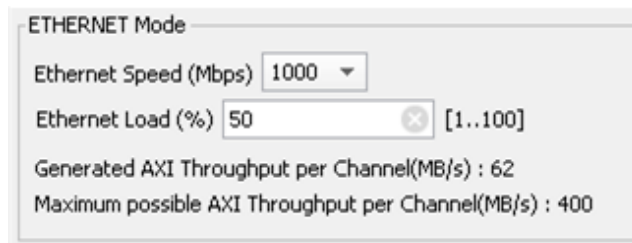


Figure 2: ATG8 – Ethernet Mode

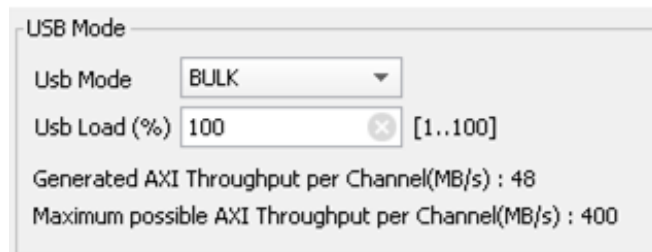


Figure 3: ATG9 – USB Mode

VIDEO Mode

Hsize: 1920 [640..1920]

Vsize: 1080 [480..1080]

Frame Rate: 60

Pixel Bits: 8

Format: RGB

Generated AXI Throughput per Channel(MB/s) : 373

Maximum possible AXI Throughput per Channel(MB/s) : 400

Figure 4: ATG10 – Video Mode

PCIe Mode

PCIe Lanes: 1

PCIe Lane Rate (GT/s): 2.5

PCIe Load(%): 50 [1..100]

Generated AXI Throughput per Channel(MB/s) : 125

Maximum possible AXI Throughput per Channel(MB/s) : 400

Figure 5: ATG11 – PCIe Mode

Each of these configuration places a specific load on the interconnect and memory. The web server application shows if these IP cores are able to get the desired bandwidth from the system. You can analyze the system characteristics and the overheads if any.

This subsystem is useful to interpret the system behavior before a real IP is available and addresses any system-level issues.

## Advanced and Stream Mode

This subsystem consists of two ATGs. ATG12 is configured in Advanced mode. This mode allows you to configure different RAMs in ATG to generate desired traffic profile. For example, the configurations can include:

- Various lengths of transactions
- Delay between two transactions
- Dependency between transactions

ATG13 is configured in Master Only Stream mode which generates streaming traffic as a master. This stream traffic is routed to DDR through AXI-DMA which takes in AXI4-Stream traffic and generates AXI4 traffic.

Table 2: Demonstration System Cores and Addresses

Core	Base Address	High Address
APM_1	0x44A00000	0x44A0FFFF
ATG_0	0x44A10000	0x44A1FFFF
ATG_1	0x44A20000	0x44A2FFFF
ATG_2	0x44A30000	0x44A3FFFF
ATG_3	0x44A40000	0x44A4FFFF

Table 2: Demonstration System Cores and Addresses (Cont'd)

Core	Base Address	High Address
ATG_4	0x44A50000	0x44A5FFFF
ATG_5	0x44A60000	0x44A6FFFF
ATG_6	0x44A70000	0x44A7FFFF
APM_2	0x44A80000	0x44A8FFFF
APM_4	0x44A90000	0x44A9FFFF
DDR	0x80000000	0xBFFFFFFF
APM_3	0x44AA0000	0x44AAFFFF
ATG_12	0x44000000	0x44ABFFFF
ATG_13	0x44AC0000	0x44ACFFFF
DMA	0x41E00000	0x41E0FFFF

**Note:** ATG8 to ATG11 does not have an AXI4 slave interface to configure. These cores start generating traffic based on external inputs `core_ext_start` and `core_ext_stop`.

## System Performance Summary

ATGs Configuration: 32-bit at 100 MHz clock

Interconnect Configuration: 256-bit at 100 MHz clock

Memory Configuration: 64-bit at 400 MHz clock

## Memory Performance Mode

Table 3 shows the throughput achieved by each ATG for Read and Write channel and throughput variation with corresponding burst length configuration. The maximum memory throughput is 6.4 GB and maximum achieved throughput is 4.8 GB (75% of DDR bandwidth).

Table 3: ATG for Read and Write Channel and Throughput

IP	Idle Throughput	Burst Length	System Throughput	
			Write	Read
ATG_0	400 MB/s x2	0x1F	360	170
ATG_1	400 MB/s x2	0x3F	370	340
ATG_2	400 MB/s x2	0x7F	390	385
ATG_3	400 MB/s x2	0xFF	395	390
ATG_4	400 MB/s x2	0x1F	360	170
ATG_5	400 MB/s x2	0x3F	370	340
ATG_6	400 MB/s x2	0x7F	390	385
Total System Throughput (6,400 MB/s)	2,800x2 = 5600 MB/s (Read + Write)		= 4,815 MB/s (Read + Write)	

## High Level Traffic Profile Mode

Table 4 shows the throughput achieved with ATG High Level Traffic Profile mode options.

Table 4: ATG High Level Traffic Profile Mode Options

IP	ATG Mode	Expected Throughput	System Throughput	
			Write	Read
ATG_8	Ethernet	62 MB x2	62	62
ATG_9	USB	48 MB x1	0	48
ATG_10	Video	373 MB x2	373	320
ATG_11	PCI	125 MB x2	125	125

## Software Application

The software application allows you to switch between subsystems available in the reference design and finer control options in each of the subsystem. Application-level software for controlling the system is written in C.

The application software in the reference design performs these actions:

1. The system, UART, and Ethernet Lite are initialized.
2. Web server related initialization is performed.
3. Memory performance mode subsystem is enabled.

After the initial setup sequence, you can enter an "?" option through HyperTerminal to get the main help menu.

### Application Menu

The software application provides a Main menu to switch between the different subsystems described in the following and submenu to each of the subsystem.

On the UART terminal Main menu is displayed when you enter "?" at the command prompt.

M = Memory Performance Mode  
H = High Level Traffic Profile (HLTP) Mode  
A = Advanced and Stream Mode  
G = Get Current Mode and Status  
? = Help

Enter a character based on the mode of interest. A detailed submenu is displayed in each mode based on the subsystem selected.

### Memory Performance Mode: Submenu

Memory Performance Mode Menu  
a = All ATGs to Minimum Length of 0xF  
b = All ATGs to Maximum Length of 0xFF  
c = Increasing Order of Lengths  
d = Decreasing Order of Lengths  
e = Arbitrary Value of 0x3F  
? = Help

In this mode, choose different available options to program the lengths of each ATG source like setting all ATGs to a minimum length of 0xF or to 0xFF, and etc.

### High Level Traffic Profile (HLTP) Mode: Submenu

High Level Traffic Profile (HLTP) Menu

f = HLTP-Start

g = HLTP-Stop

? = Help

In this mode, choose to enable or disable all HLTP cores in the subsystem.

### High Level Traffic Profile (HLTP) Mode: Submenu

Advanced and Stream Menu

h = AXI4 Transactions with Fix Length of 0x1

i = AXI4 Transactions with Fix Length of 0xFF

j = AXI4 Transactions with Variable Length of 0x0 to 0xFF

? = Help

In this mode, choose to set the lengths of transactions generated using Advanced mode of ATG.

**Note:** Any time during the run, you can enter "?" to get the Main Menu.

### SDK Options

To link a web server application to SDK c-application, the following settings are needed:

1. The settings are completed in application properties to point to pre-compiled web server image files (right-click **Application** in SDK project and select **Properties**) See [Figure 6](#).



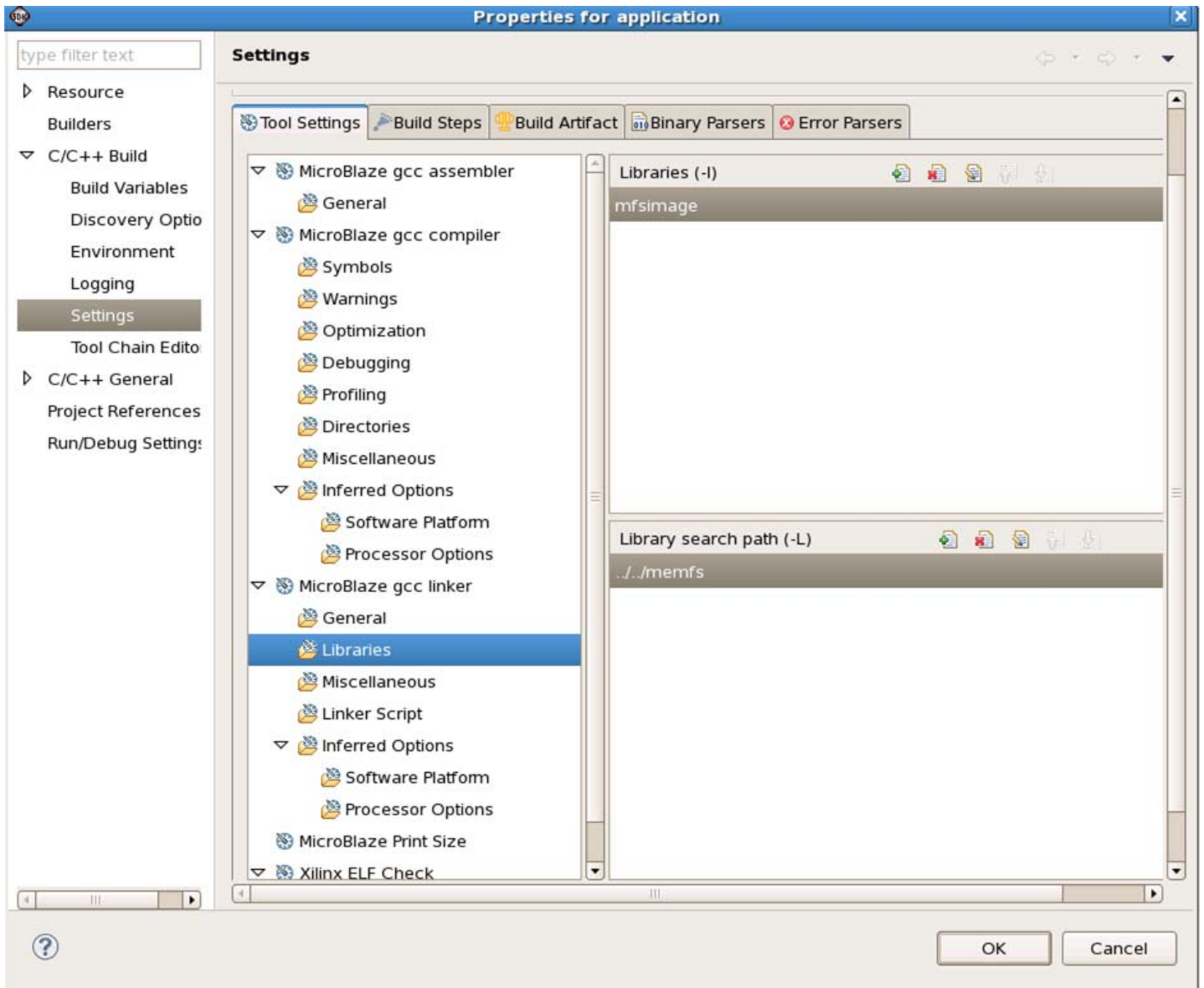


Figure 6: Properties for Application

2. The settings are completed under xilkernel bsb (right-click xilkernel\_bsp\_0 in SDK project and select **Board Support Package Settings**). See [Figure 7](#).

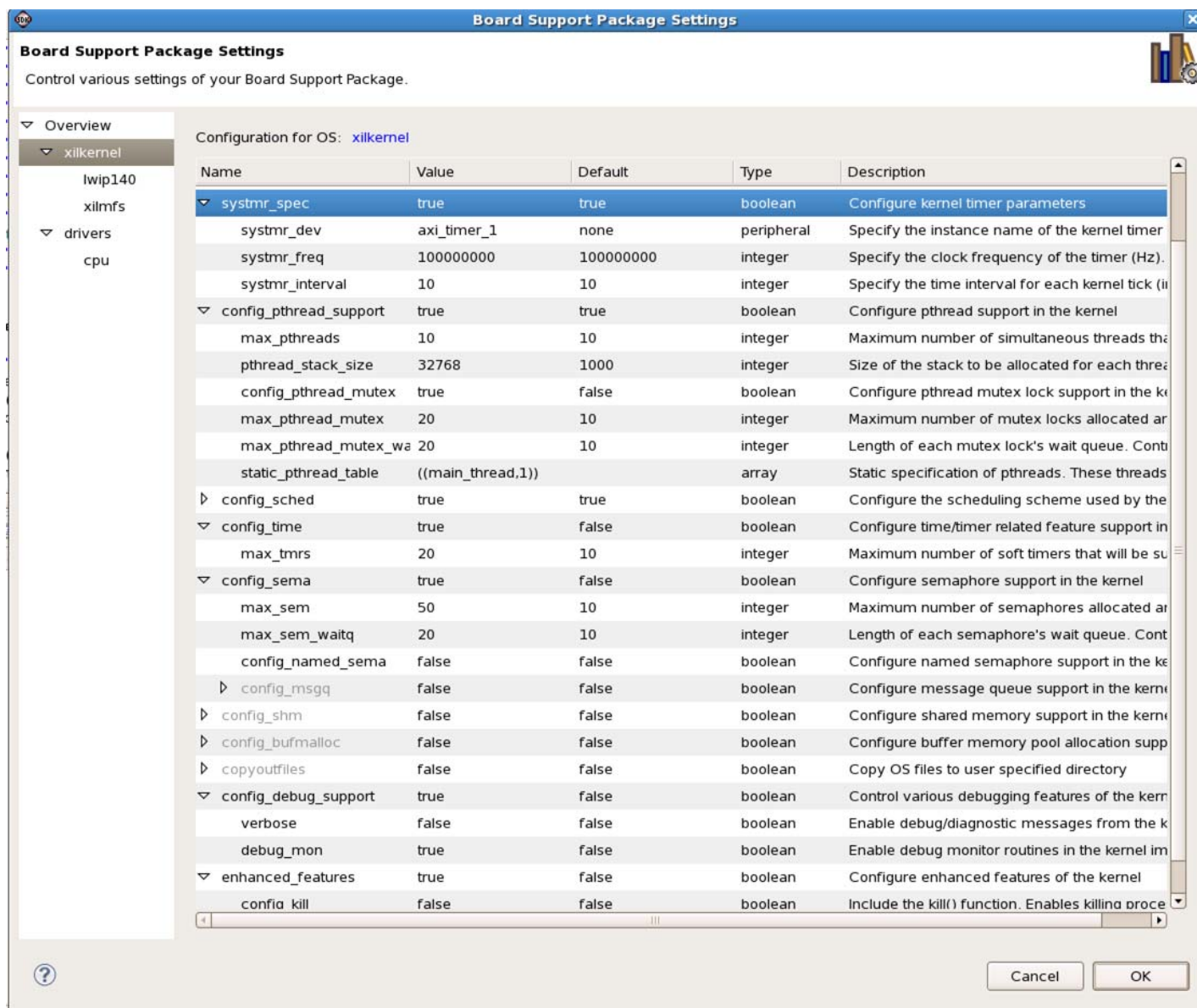


Figure 7: Board Support Package Settings

Follow these steps to set up the system.

1. Connect a USB cable from the host PC to the USB JTAG port (item 6 in [Figure 8](#)). Ensure that the appropriate device drivers are installed (for additional information, see the *Kintex-7 FPGA KC705 Evaluation Kit Getting Started Guide* (UG883) [[Ref 2](#)]).
2. Connect a second USB cable from the host PC to the USB UART port (near item 6 in [Figure 8](#)). Ensure that the USB-UART drivers described in [Hardware and Software Requirements, page 2](#) have been Installed.
3. Connect a power supply cable.
4. Turn the power on (item 27).
5. Start a terminal program (for example, HyperTerminal) on the host PC with these settings:
  - Baud rate: 9600
  - Data bits: 8
  - Parity: None
  - Stop bits: 1

- Flow control: None

## Executing the Reference Design on Hardware

This section provides instructions on executing the reference design in hardware. The reference design runs on the KC705 board shown in [Figure 8](#). In these instructions, numbers in parentheses correspond to the callout numbers in [Figure 8](#). Not all callout numbers are referenced.

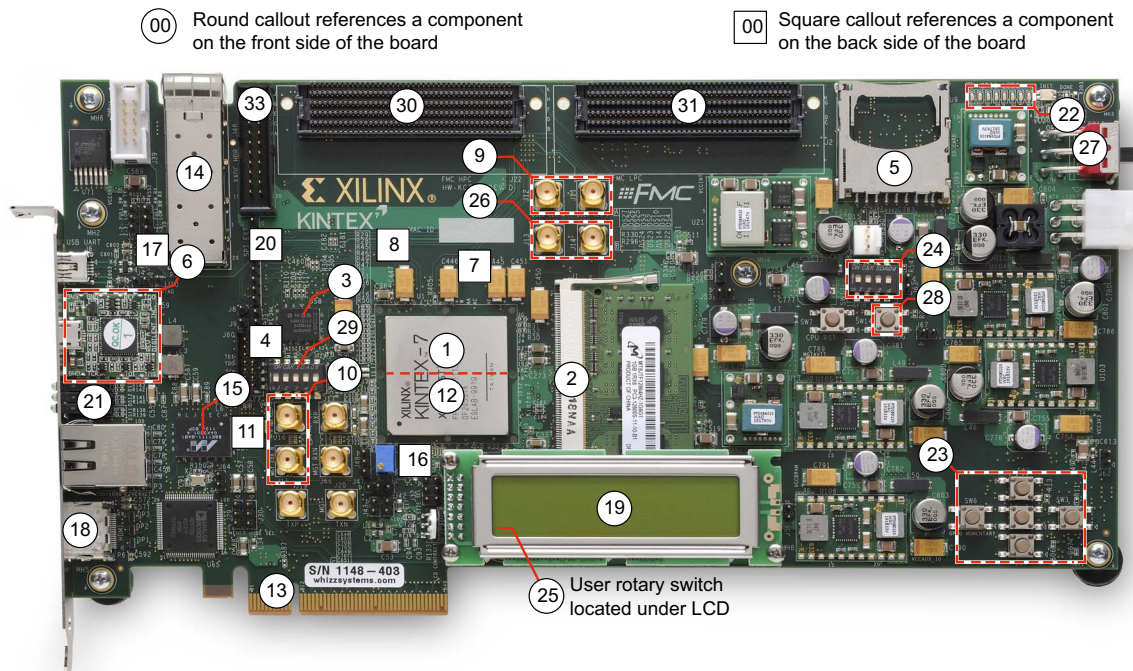


Figure 8: KC705 Board

### Executing the Reference System Using the Pre-Built Bitstream and the Compiled Software Application

These are the steps to execute the system using the files in the `ready_for_download` directory of the `<unzip_dir>/xapp1202` directory.

1. Connect the Ethernet cable between the KC705 board and the Host machine. Configure the Host machine Ethernet card for 100 Mb/s full duplex.
2. In a Xilinx command shell (Vivado Design Suite 32/64-bit command prompt) or terminal window, change the directories to the `ready_for_download` directory.

```
% cd <unzip_dir>/xapp1202/ready_for_download
```

3. Invoke the Xilinx Microprocessor Debugger (XMD) tool:

```
% xmd
```

4. Download the bitstream inside the XMD:

```
XMD% fpga -f download.bit
```

5. Connect to the processor inside the XMD:

```
XMD% connect mb mdm
```

6. Download the processor code (ELF) file:

```
XMD% dow application.elf
```

7. Run the software:

```
XMD% run
```

8. In Host PC, configure the ethernet address to 192.168.1.1 by following the instructions. Click **Start > Control Panel > Network and Sharing Center > Change Adaptor Settings**. Right-click **Local Area Connections** and select **Properties**. Click **Yes** and double-click **Internet Protocol version 4 (TCP/IPv4) > Change the IP Address** and press **OK**.
  9. Go to the Host machine and type IP address 192.168.1.10 (web server address).
- Note:** Ensure that the similar image shown in Figure 9 (for example, seven different graphs) is displayed. Initially, all of the graphs do not have any plots until **Start Benchmark** button is clicked. Best viewed in Mozilla® Firefox® version 26.0 and higher.

## Results for Running Hardware and Software Systems

Figure 9 and Figure 10 show the web browser page after loading the application.



Figure 9: ATG and APM Demonstrations Web Browser Page

Web page contains user options to select the desired subsystem to run and top-level controls in each mode. The source of metrics for the first four graphs varies based on the mode selected. The table at the bottom of the web page lists these sources with respect to mode. The last three graphs display DDR metrics of Read and Write throughput, utilization, and average latency numbers. All of the APMs are configured to sample metrics for a window of 500 ms. The application also plots the graphs with new values at an interval of 500 ms.

**ATG-APM Demonstration**

**Legends**

-->Write Channel

-->Read Channel

--> Utilization

--> DDR Max Throughput

**User Options**

**Steps to RUN** (a)Select Mode (b)Click Start Benchmark Graph (c)Click Stop Benchmark Graph (d)Goto Step(a)

**Mode**  Memory Performance Mode  High Level Traffic Profile Mode  Advanced & Stream Mode

**Memory Performance Mode Controls**

ATG set-0 <input checked="" type="radio"/> 0xF <input type="radio"/> 0x1F <input type="radio"/> 0x3F <input type="radio"/> 0x7F <input type="radio"/> 0xFF	ATG set-1 <input checked="" type="radio"/> 0xF <input type="radio"/> 0x1F <input type="radio"/> 0x3F <input type="radio"/> 0x7F <input type="radio"/> 0xFF
ATG set-2 <input checked="" type="radio"/> 0xF <input type="radio"/> 0x1F <input type="radio"/> 0x3F <input type="radio"/> 0x7F <input type="radio"/> 0xFF	ATG set-3 <input checked="" type="radio"/> 0xF <input type="radio"/> 0x1F <input type="radio"/> 0x3F <input type="radio"/> 0x7F <input type="radio"/> 0xFF

**High Level Traffic Profile Mode Controls**

HLTP  Enable  Disable

**Advanced&Stream Mode Controls**

Advanced  Enable  Disable      Stream  Enable  Disable

*Note: For finer controls please use c-application menu*

Figure 10: Web Page Control Options

- **Legends** – On all of the graphs displayed in web page, specific color coding is used to differentiate metrics.
    - Red color lines indicate write channel characteristics.
    - Green color lines indicate read channel characteristics.
    - Brown color lines indicate bandwidth utilization numbers.
    - Gray color lines indicate maximum throughput possible with current DDR settings.
  - **Steps to RUN** – Quick instructions for the sequence of steps to run this application.
  - **Mode** – Select one of the three modes to analyze the system behavior.
  - **Memory Performance Mode Controls** – Set burst length for each set of ATG to one of the available options 0xF, 0x1F, 0x3F, 0x7F, or 0xFF.
  - **High Level Traffic Mode Controls** – Either disable all the ATGs to stop generating traffic or enable all the ATGs to start generating IP specific traffic.
  - **Advanced and Stream Mode Controls** – Either enable or disable Advanced and stream ATGs individually.
- Note:** There are more fine grain options available under each mode through c-application menu.

## Memory Performance Mode Demonstration Run

Seven ATGs available in this system are divided into the following four sets:

- ATG0, ATG4 form set-0
- ATG1, ATG5 form set-1
- ATG2, ATG6 form set-2
- ATG3 form set-3

Each set can be configured to generate specific burst lengths.

1. Select **Memory Performance Mode**.
2. Select **Burst Lengths** for each ATG set.
3. Click **Start Benchmark Graph**.
4. From the c-application menu, vary the lengths dynamically if desired for each ATG set using the options provided (for example, configuring all ATGs to minimum length).
5. Observe and analyze graphs.
6. Click **Stop Benchmark Graph**.

Figure 11 to Figure 13 show the example run with 0x1F, 0x3F, 0x7F, and 0xFF burst lengths configured for each ATG sets.

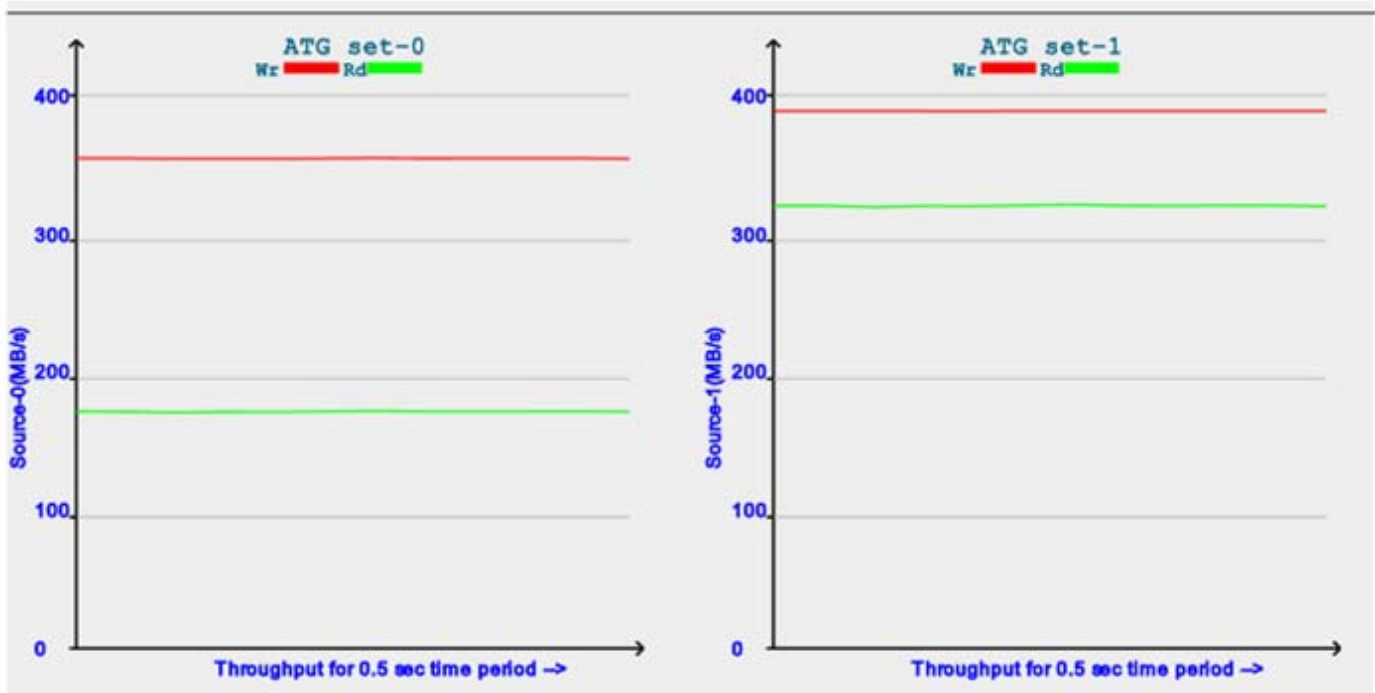


Figure 11: Memory Performance Mode – ATG Set-0 and ATG Set-1

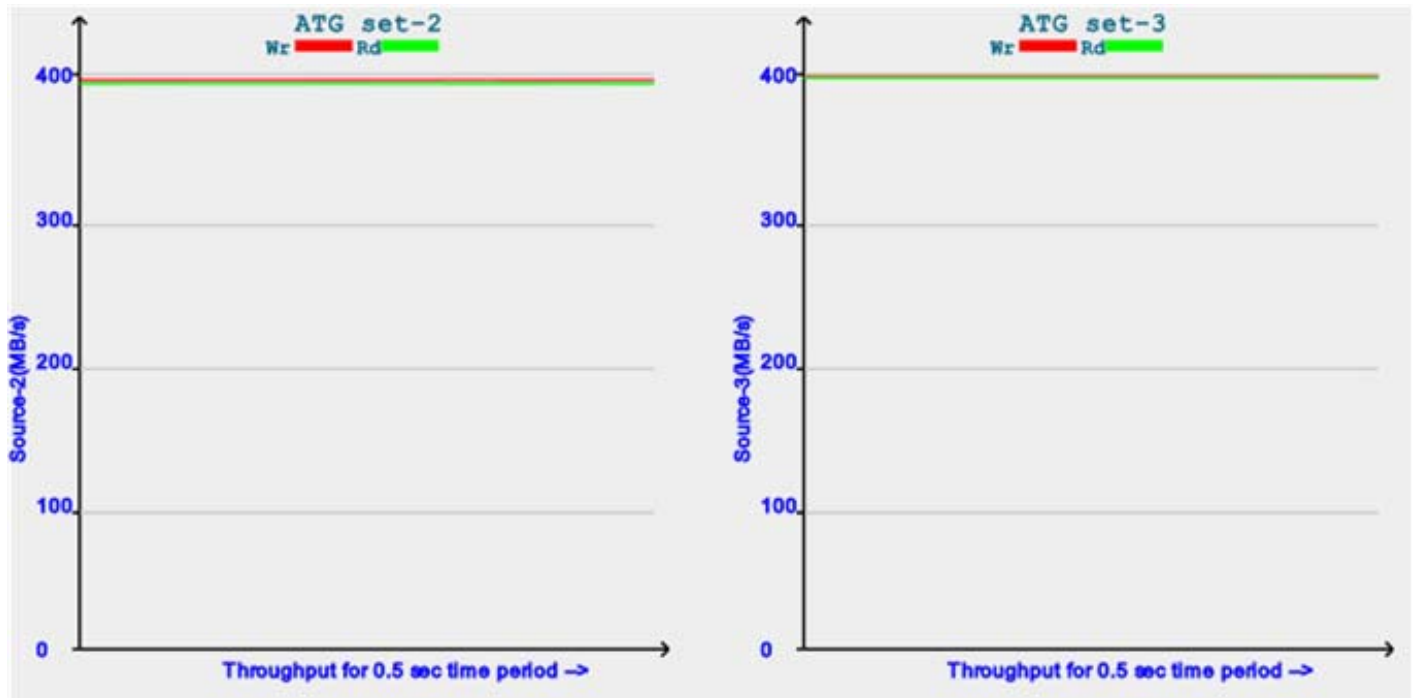


Figure 12: Memory Performance Mode – ATG Set-2 and ATG Set-3

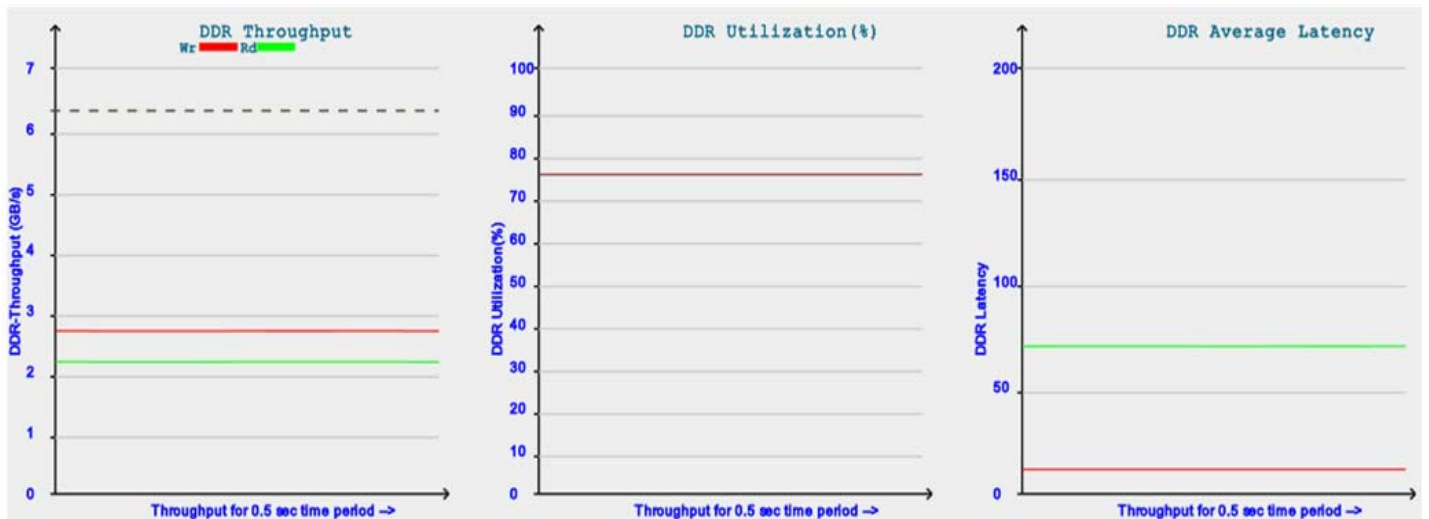


Figure 13: Memory Performance Mode – DDR

### Inference

In Figure 11 and Figure 12, the throughput graphs of ATG set-0, ATG set-1, ATG set-2, and ATG set-3, there is a huge throughput advantage for a core with burst length of 0xFF versus 0x1F and only little throughput advantage (of order of 1 MB/s) with burst lengths of 0x7F and 0xFF.

Varying the burst lengths generated from each ATG source greatly helps you to analyze and arrive at the optimum configurations for the core.

In Figure 13, you can evaluate the metrics at the target memory. You can also analyze how effectively the target memory is used in the current system and the opportunities available to use its full capacity.

Write throughputs are a little higher than the read throughput and this matches with DDR latency numbers reported where the read latency is higher in the system than the write latency.

## High Level Traffic Profile Mode Demonstration Run

Four ATGs available in this system are configured to generate IP specific traffic profiles.

1. Select **High Level Traffic Profile Mode**.
2. Click **Start Benchmark Graph**.
3. Observe and analyze graphs.
4. Click **Stop Benchmark Graph**.

Figure 14 to Figure 16 show the example run for this mode.

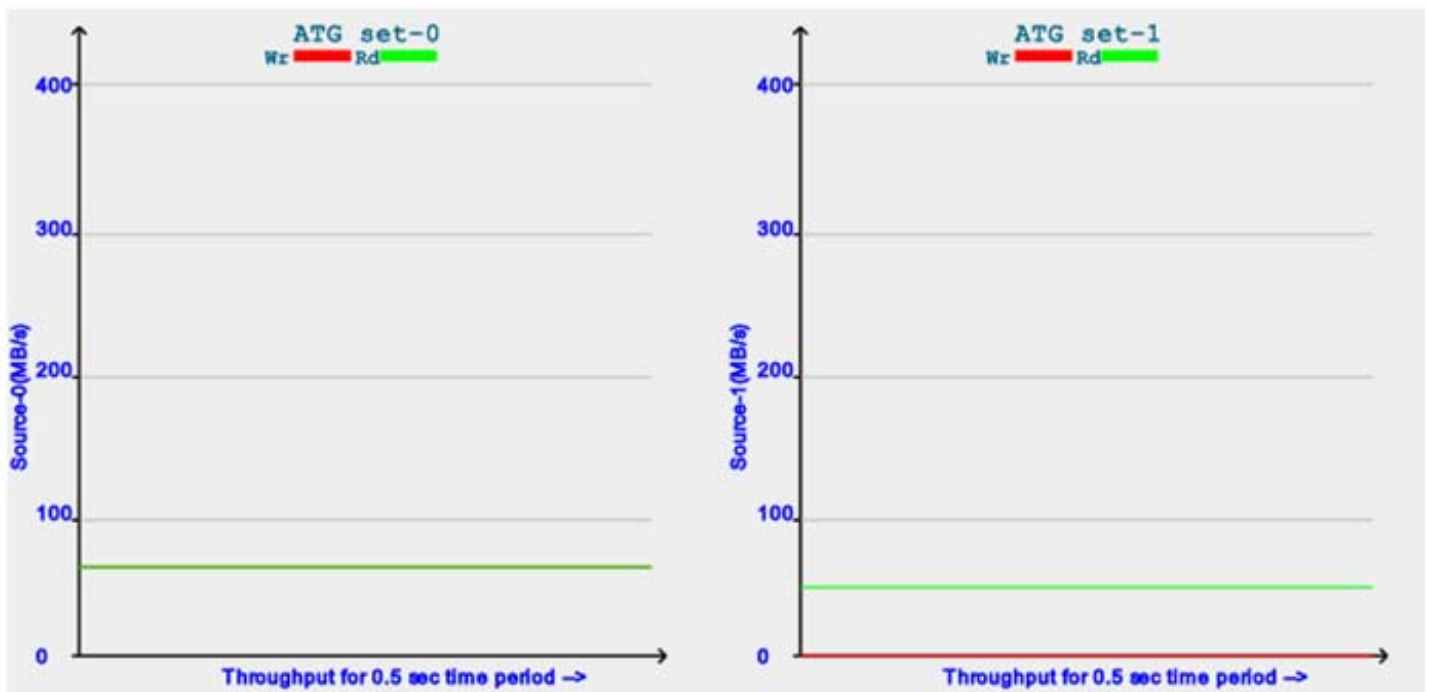


Figure 14: High Level Traffic Profile Mode – ATG Set-0 and ATG Set-1



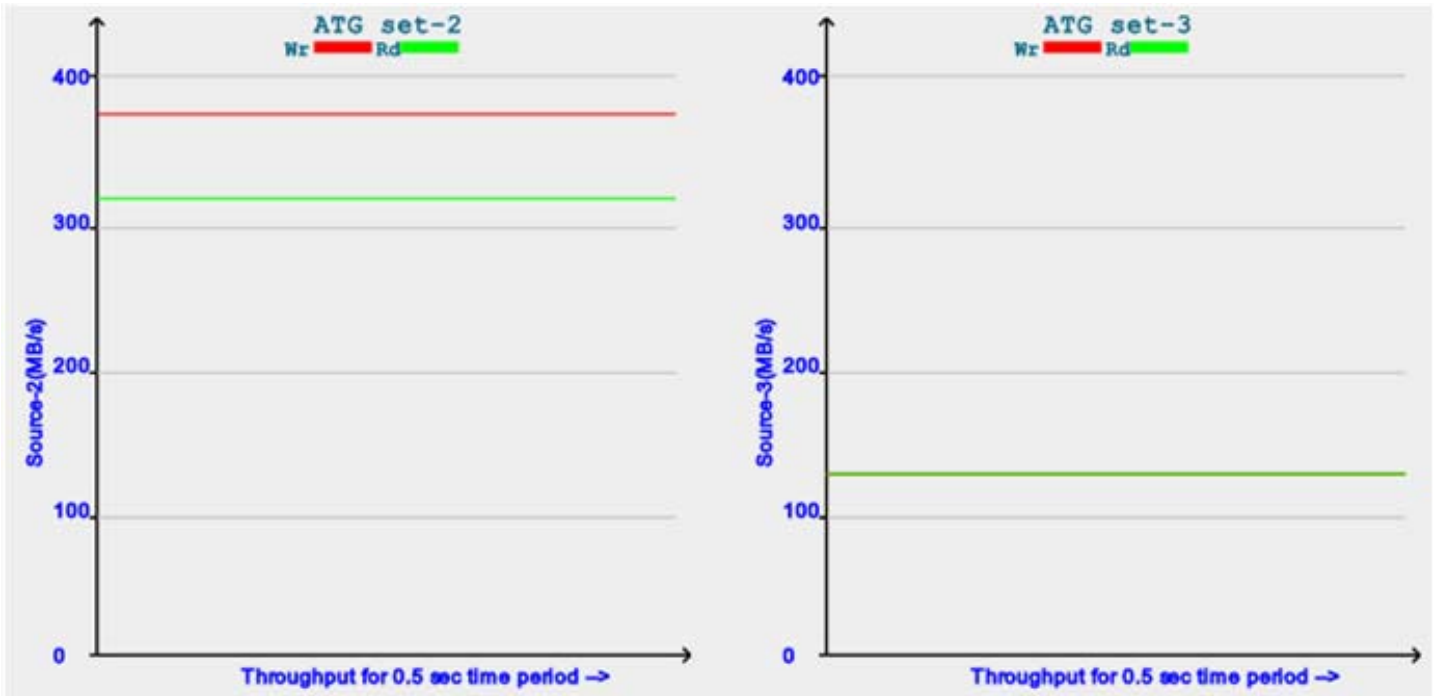


Figure 15: High Level Traffic Profile Mode – ATG Set-2 and ATG Set-3

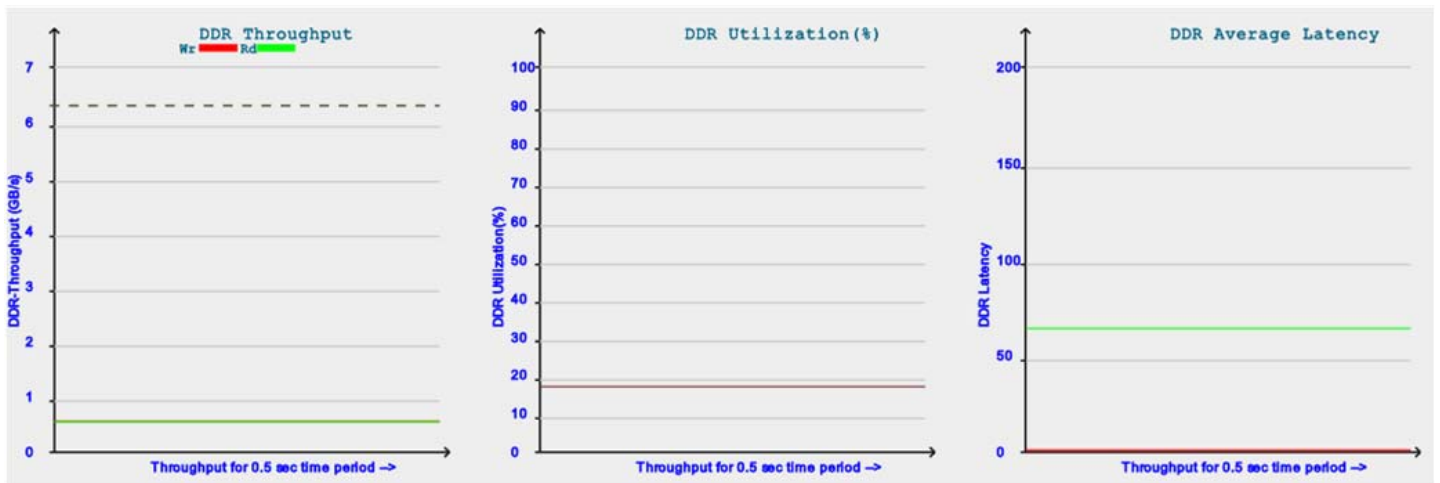


Figure 16: High Level Traffic Profile Mode – DDR

### Inference

Each ATG source is configured to mimic AXI4 throughput of pre-defined protocols Ethernet, USB, Video, and PCIe.

See [High Level Traffic Profile Mode, page 4](#) for ATG configurations and expected AXI4 throughput numbers.

USB traffic reported on ATG set-1 shows that the write throughput is zero. This is because a USB core can either be a read or write at a time and the current configuration is set to generate read traffic.

The read and write throughput seen at DDR is almost equal in this case.

**Note:** Dark green in set-0 and set-3 is due to red and green lines drawn at the same point.

Now you can replace any of the ATGs with the real IP cores in the system and expect a similar behavior at the AXI4 side of the IP. This helps you receive the system-level characteristics before the actual IP is in place.

## Advanced and Stream Mode Demonstration Run

Two ATGs available in this system are configured to generate user-defined traffic profile and stream traffic.

1. Select **Advanced and Stream Mode**.
2. Click **Start Benchmark Graph**.
3. From the c-application menu, vary the configurations of ATGs based on the options provided.
4. Observe and analyze graphs.
5. Click **Stop Benchmark Graph**.

Figure 17 and Figure 18 show the example run for this mode.

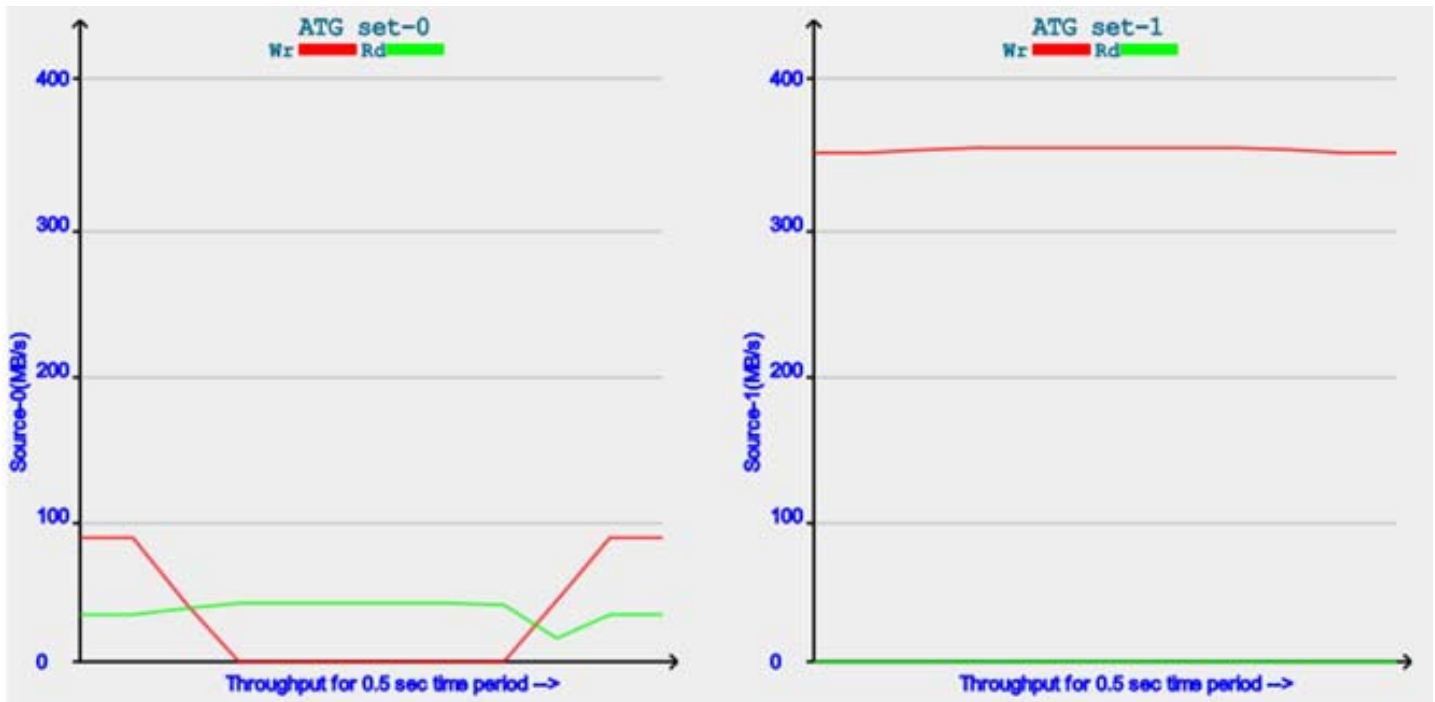


Figure 17: Advanced and Stream Mode – ATG Set-0 and ATG Set-1

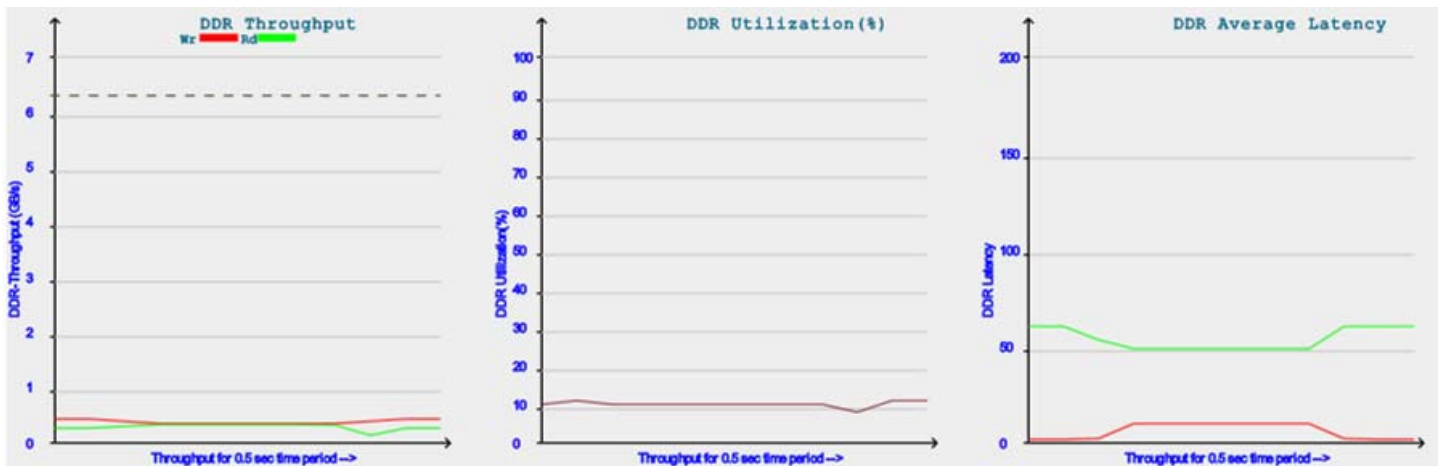


Figure 18: Advanced and Stream Mode – DDR

### Inference

In Figure 17, ATG set-0 plots metrics from Advanced mode of ATG. Based on the transactions programmed to `cmdram`, the graphs show a variation in read and write throughput.

Variation at ATG set-0 reflects on Figure 18 by decreasing write throughput and slight increase in read throughput.

As the Stream ATG is in Master Only mode, this only generates a write traffic. This can be seen in ATG set-1 graph that read throughput is always reports 0.

## Reference Design Details

The reference design has been fully verified and tested on hardware. The design includes details on the various functions of the different modules. The interface has been successfully placed and routed at 100 MHz on the main AXI4 Interfaces to the memory controller using the Vivado Design Suite 2013.4.

[Click here](#) to download the design files associated with this application note.

Table 5 shows the reference design matrix.

Table 5: Reference Design Matrix

Parameter	Description
<b>General</b>	
Developer name	Kondalarao Polisetti, Pankaj Kumbhare
Target devices	Kintex-7 FPGAs
Source code provided	Yes
Source code format	VHDL/Verilog
Design uses code/IP from existing Xilinx application note/reference designs, Vivado design tools, or third-party	N/A
<b>Simulation</b>	
Functional simulation performed	N/A
Timing simulation performed	N/A
Test bench used for functional and timing simulations	N/A
Test bench format	N/A

Table 5: Reference Design Matrix (Cont'd)

Parameter	Description
Simulator software/version used	N/A
SPICE/IBIS simulations	N/A
<b>Implementation</b>	
Synthesis software tools/version used	Vivado Design Suite 2013.4
Implementation software tools/versions used	Vivado Design Suite 2013.4
Static timing analysis performed	Yes (Timing passed with Vivado Design Implementation)
<b>Hardware Verification</b>	
Hardware verified	Yes
Hardware platform used for verification	KC705 Revision 1.1 board

Table 6: Performance and Utilization

Component	Value
<b>Slice Logic</b>	
Slice LUTs	106,604 (53%)
Slice Registers	79,871 (20%)
<b>IOBs</b>	
I/Os	138 (27%)
<b>Memory</b>	
RAMB36E1s	207 (46%)
RAMB18E1s	137 (15%)
<b>Clocking</b>	
BUFGCTRL	6 (18%)
MMCME2_ADV	1 (10%)
PLLE2_ADV	1 (10%)
<b>General</b>	
Run Time	100 minutes
Timing Violations	None

Table 7: Module Level Utilization

Instance	Total LUTs	FFs	RAMB36	RAMB18
Top	106,604	79,871	207	137
Memory Performance mode	27,532	17,173	65	17
HLTP mode	22,383	14,577	35	34
Adv_Streaming_mode	20,994	15,834	29	39
APM_4	8,045	4,603	0	7
IC_11	7,224	9,116	62	40
microblaze_1	1,854	1,613	10	0

Table 7: Module Level Utilization (Cont'd)

Instance	Total LUTs	FFs	RAMB36	RAMB18
mig_1	13,198	10,550	0	0
axi_ethernetlite_0	634	620	4	0
axi_intc_1	261	233	0	0
axi_interconnect_1	4,112	5,136	0	0
axi_timer_1	256	213	0	0
axi_uartlite_1	99	90	0	0
blk_mem_gen_1	0	0	2	0
lmb_bram_if_cntlr_1	6	2	0	0
lmb_bram_if_cntlr_2	2	2	0	0
lmb_v10_1	0	1	0	0
lmb_v10_2	0	1	0	0
mdm_1	31	76	0	0
proc_sys_reset_1	18	31	0	0

**Note:** The utilization information is approximate due to cross-boundary logic optimizations and logic sharing between modules.

## References

1. [ARM® AMBA® AXI Protocol Specification](#), version 2.0 (ARM IHI 0022C)
2. *Kintex-7 FPGA KC705 Evaluation Kit Getting Started Guide* ([UG883](#))
3. *LogiCORE™ IP AXI Traffic Generator Product Guide* ([PG125](#))
4. *LogiCORE IP AXI Performance Monitor Product Guide* ([PG037](#))
5. *LogiCORE IP AXI Interconnect Product Guide* ([PG059](#))
6. *AXI Reference Guide* ([UG761](#))
7. *Vivado Design Suite User Guide: Designing IP Subsystems Using IP Integrator* ([UG994](#))
8. *Vivado Design Suite Tutorial: Designing IP Subsystems Using IP Integrator* ([UG995](#))

## Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
02/26/2014	1.0	Initial Xilinx release.

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